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BYG43

Lenovo Yoga 700 (14)

NM-A601 REV1.0

Haydn SKL M/B Schematics Document

INTEL SKYLAKE-U Platform
INTEL SKL U-series CPU + DDR3L DIMM+ NV N16S-GT

2015-07-20

REV:1.0

Security Classification	LC Future Center Secret Data		
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Title		
Cover Page		
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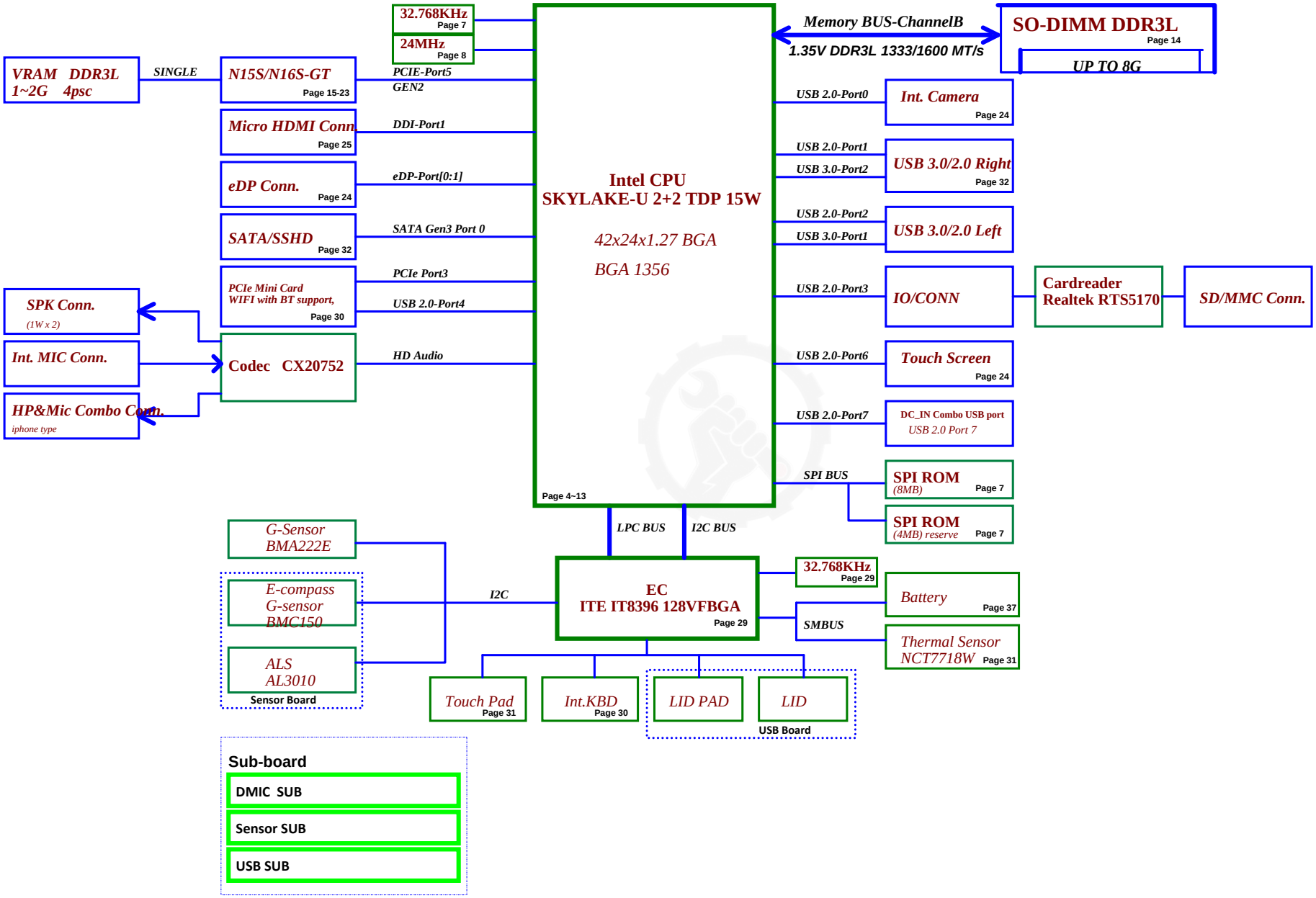
Yoga 700(14) Block diagram



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Title: Block Diagram

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Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State	B+ +3VL +5VLP	+3VALW +5VALW	+3VALW_PCH	+1.35V	+5VS +3VS +1.5VS +1.05VS +0.68VS +CPU_CORE	+1.35V_CPU
S0	O	O	O	O	O	O
S3	O	O	O	O	X	O
DS3	O	O	X	O	X	X
S5 S4/AC Only	O	O	O	X	X	X
S5 S4 Battery only	O	X	X	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X	X	X

STATE / SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	+VALW	+VALW_PCH	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	ON	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	ON	ON	ON	OFF	OFF
DS3 (Suspend to RAM)	LOW	LOW	HIGH	ON	LOW	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	ON	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	ON	OFF	OFF	OFF

SMBUS Control Table

	SOURCE	Sensor	ALS	BATT	touch sensor	SODIMM	GPU	Thermal Sensor	PCH	charger
EC_SMB_CLK1 EC_SMB_DAT1	IT8386 +3VALW_EC	X	X	V +3VLP	X	X	X	X	X	V
EC_SMB_CLK3 EC_SMB_DAT3	IT8386 +3VS	V +3VS	V +3VS	X	X	X	X	X	X	X
EC_SMB_CLK0 EC_SMB_DAT0	IT8386 +3VS	X	X	X	X	X	V	V +3VS	V +3VALW_PCH	X
SMB_CLK SMB_DATA	PCH +3VALW_PCH	X	X	X	X	V +3VS	X	X	X	X

SM Bus address

	Device	address
EC1	Battery	0001 011X b
	Charger	
EC3	Sensor	
	ALS	
EC0	Thermal Sensor	1001_100xb
	PCH THM	
PCH	TP	

PCIE PORT LIST

Port	Device
1	X
2	X
3	WLAN
4	X
5	GPU

USB Port Table

	USB20		USB30	
EXHCI/XHCI	0	CAMERA	1	Left USB
	1	Right USB	2	Right USB
	2	Left USB	3	X
	3	CARD READER	4	X
	4	BT		
	5	Sensor		
	6	TOUCH PANEL		
	7	DC_IN combo USB2.0		

BOM Structure Table

BOM Structure		BOM Structure	
DA8@	PCB	MIRROR@	EC Mirror-code enable
UMA@	UMA SKU part	UNMIRROR@	EC Mirror-code disableable
DEBUG@	DEBUG CARD Part	OPT@	Discrete GPU SKU part
ME@	ME part(connector, hole)	N15SGT@	For N15S-GT GPU part
RF@	RF request	GC6@	GC62.0 support part
EMC@	EMC request	RANKA@	For VRAM RankA part
CD@	COST DOWN Part		
REV@	RESERVER Part		

Board ID Table

Board ID	Description	PCB Revision

BOM Configuration Table

SKU	Description	BOM Config	
SKU1			
SKU2			

X76&VGA Configuration Table

SKU	Description	BOM Config	

PCB And LOGO Config

PCB	ZZZ3 DA8@ PCB BYG43 NM-A601 NS-A601/A602	LOGO
CPU	ZZZ1 2.3G@ Intel i5-6200U 2.3G/2C/3M; ZZZ2 2.5G@ Intel i7-6500U 2.5G/2C/4M	ZZZ4 HDMI@ HDMI LOGO; ZZZ5 USB30@ USB30 LOGO
VRAM	ZZZ6 HY2G@ HYNIX 2G; ZZZ7 MIC2G@ MICRON 2G; ZZZ8 SAM2G@ SAMSUNG 2G	

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Title: Notes List

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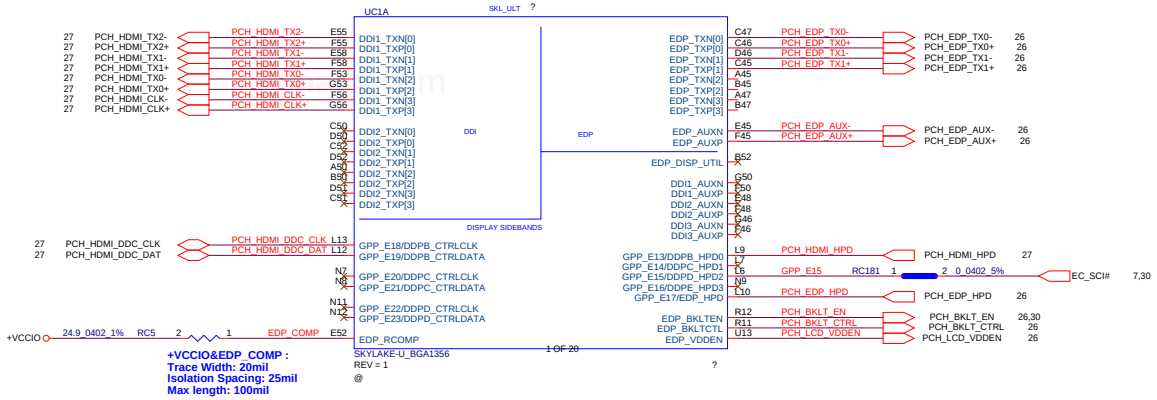
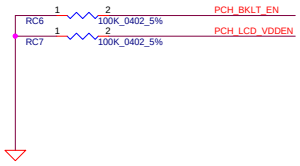
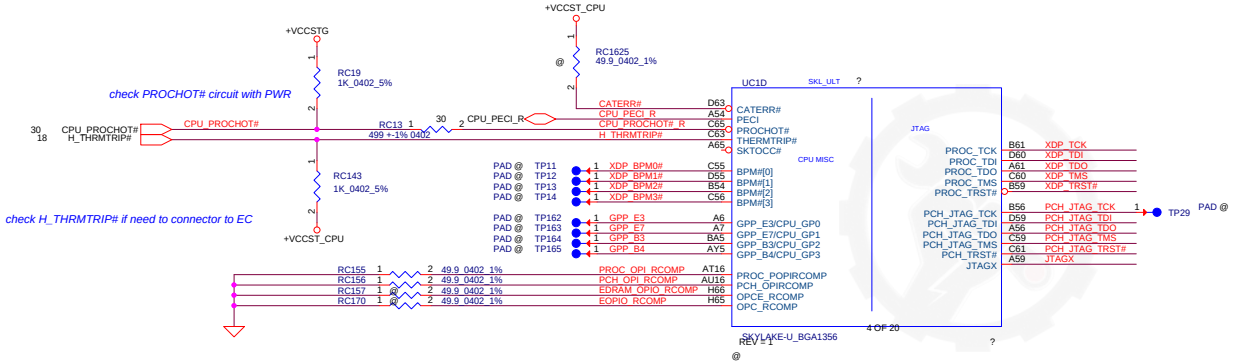
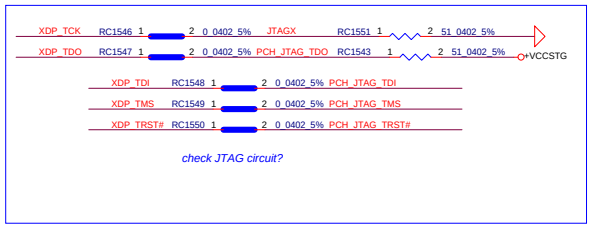


+VCCIO&EDP_COMP :
Trace Width: 20mil
Isolation Spacing: 25mil
Max length: 100mil







DDP*_CTRLDATA strapping sampled on the rising edge of PWROK

Port	Strap	Enable	Disable
Port 1	DDPB_CTRLDATA	Pull up to 3.3 V with 2.2Kohm	NC
Port 2	DDPC_CTRLDATA	Pull up to 3.3 V with 2.2Kohm	NC

Port	DDI PROCESSOR Pin Names	HDMI* Mapping
Port 1	DDI1_TXN[0]	HDMIxC_TX2_DN
	DDI1_TXP[0]	HDMIxC_TX2_DP
	DDI1_TXN[1]	HDMIxC_TX1_DN
	DDI1_TXP[1]	HDMIxC_TX1_DP
	DDI1_TXN[2]	HDMIxC_TX0_DN
	DDI1_TXP[2]	HDMIxC_TX0_DP
	DDI1_TXN[3]	HDMIxC_CLK_DN
	DDI1_TXP[3]	HDMIxC_CLK_DP
	DDPB_HPD	DDI1_HPD_Q
	DDPB_CTRLCLK	DDI1_CTRL_CK
	DDPB_CTRLDATA	DDI1_CTRL_DATA

DisplayPort* Disabling and Termination

Pin Name	Recommendation
DDPC_AUXP	No Connect
DDPC_AUXN	No Connect
DDPC_HPD	No Connect
DDI2_TXP[3:0]	No Connect
DDI2_TXN[3:0]	No Connect
DDPC_CTRLCLK	No Connect
DDPC_CTRLDATA	No Connect

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Title: **MCP (DDI,EDP)**

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SKL-U interleaved,

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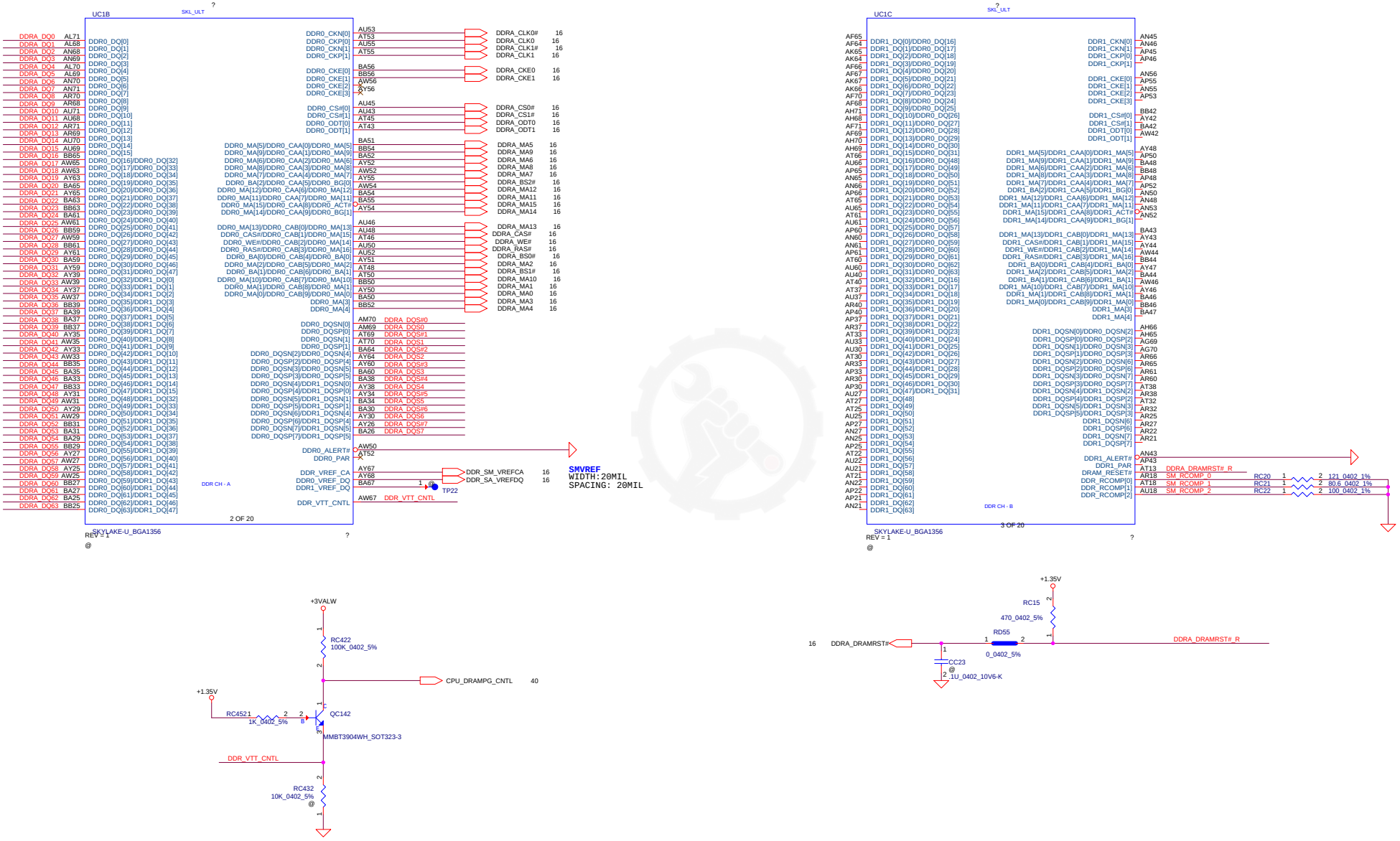
DDRA_DQ[63:0] 16
DDRA_DQS[7:0] 16
DDRA_DQS#[7:0] 16



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Title
MCP (DDR3L)

Size	Document Number	Rev
C	Haydn-S	1.0

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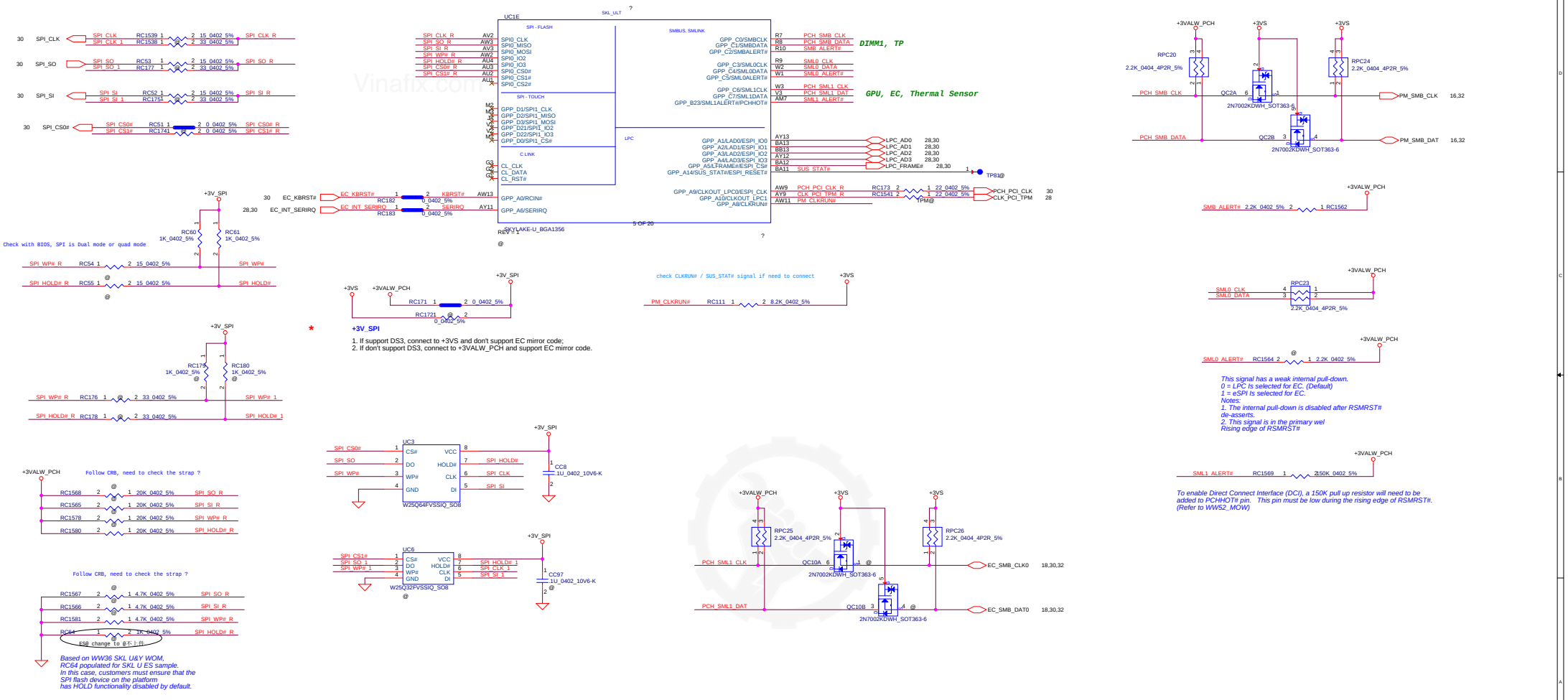

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Title: MPC (MISC,JTAG,SPI,LPC)

Size: Custom | Document Number: Haydn-S | Rev: 1.0

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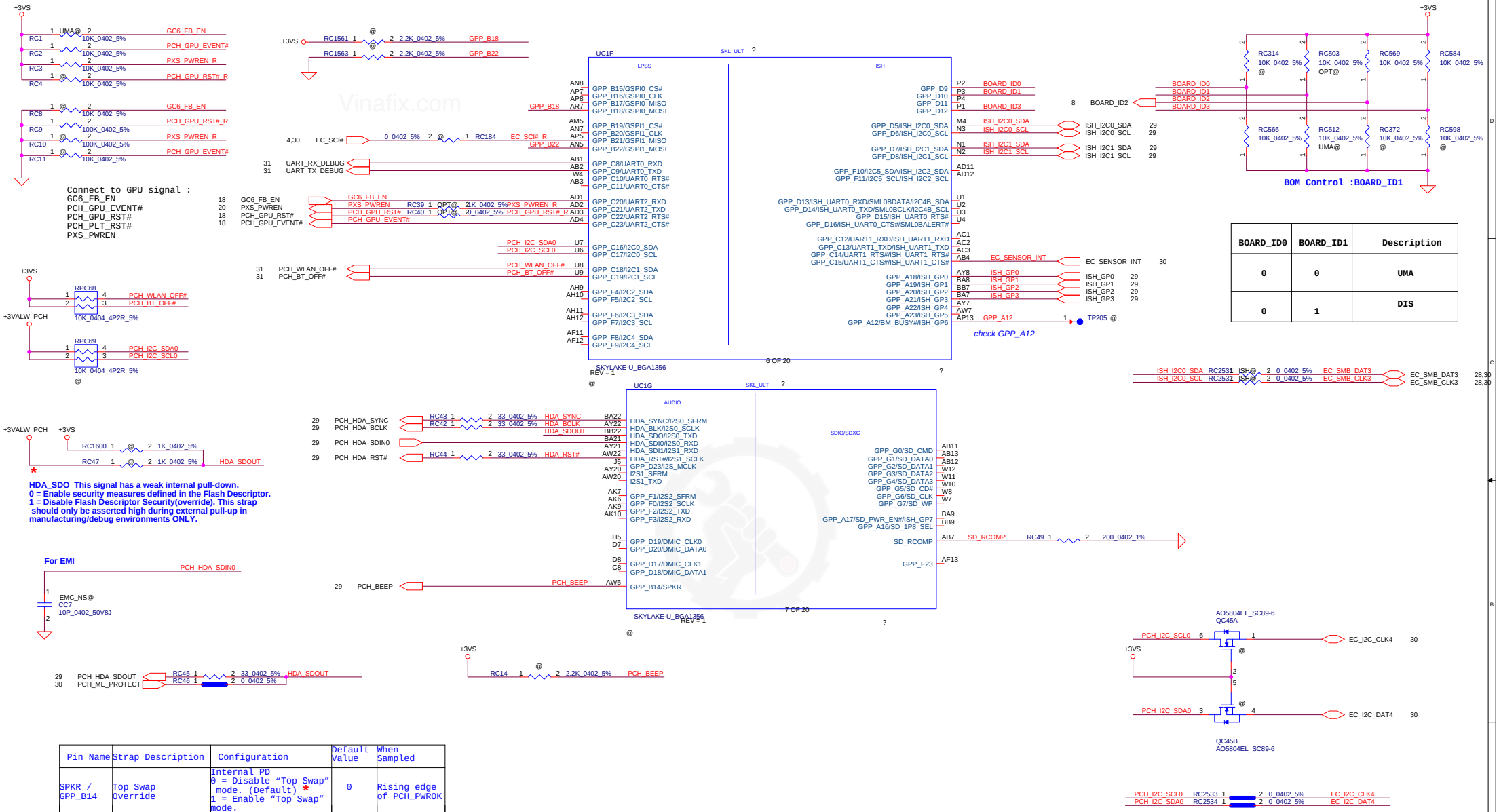

BOARD_ID0	BOARD_ID1	Description
0	0	UMA
0	1	DIS

Pin Name	Strap Description	Configuration	Default Value	When Sampled
SPKR / GPP_B14	Top Swap Override	Internal PD 0 = Disable "Top Swap" mode. (Default) * 1 = Enable "Top Swap" mode.	0	Rising edge of PCH_PWROK
GSPI0_MOSI /GPP_B18	No Reboot	Internal PD 0 = Disable "No Reboot" mode. (Default) * 1 = Enable "No Reboot" mode	0	Rising edge of PCH_PWROK
GSPI1_MOSI /GPP_B22	Boot BIOS Strap Bit BBS	Internal PD 0 = SPI (Default)* 1 = LPC	0	Rising edge of PCH_PWROK

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Title: MCP (LPSS,ISH,AUDIO,SDI

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UC1H — SKL_ULT — PCIE/USB3/SATA — SSIC / USB3 — USB2

Pin	Signal	Pin	Signal
H13	PCIE1_RXN/USB3_5_RXN	G18	PCIE6_RXN
G13	PCIE1_RXP/USB3_5_RXP	F18	PCIE6_RXP
B17	PCIE1_TXN/USB3_5_TXN	D20	PCIE6_TXN
A17	PCIE1_TXP/USB3_5_TXP	C20	PCIE6_TXP
G11	PCIE2_RXN/USB3_6_RXN	F20	PCIE7_RXN/SATA0_RXN
F11	PCIE2_RXP/USB3_6_RXP	E20	PCIE7_RXP/SATA0_RXP
D16	PCIE2_TXN/USB3_6_TXN	B21	PCIE7_TXN/SATA0_TXN
C16	PCIE2_TXP/USB3_6_TXP	A21	PCIE7_TXP/SATA0_TXP
H16	PCIE3_RXN	G21	PCIE8_RXN/SATA1A_RXN
G16	PCIE3_RXP	F21	PCIE8_RXP/SATA1A_RXP
D17	PCIE3_TXN	D21	PCIE8_TXN/SATA1A_TXN
C17	PCIE3_TXP	C21	PCIE8_TXP/SATA1A_TXP
G15	PCIE4_RXN	E22	PCIE9_RXN
F15	PCIE4_RXP	E23	PCIE9_RXP
B19	PCIE4_TXN	B23	PCIE9_TXN
A19	PCIE4_TXP	A23	PCIE9_TXP
F16	PCIE5_RXN	F25	PCIE10_RXN
E16	PCIE5_RXP	E25	PCIE10_RXP
C19	PCIE5_TXN	D23	PCIE10_TXN
D19	PCIE5_TXP	C23	PCIE10_TXP
		F5	PCIE_RCOMPN
		E5	PCIE_RCOMPP
		D56	PROC_PRDY#
		D61	PROC_PREQ#
		BB11	GPP_A7/PIRQA#
		E28	PCIE11_RXN/SATA1B_RXN
		E27	PCIE11_RXP/SATA1B_RXP
		D24	PCIE11_TXN/SATA1B_TXN
		C24	PCIE11_TXP/SATA1B_TXP
		E30	PCIE12_RXN/SATA2_RXN
		F30	PCIE12_RXP/SATA2_RXP
		A25	PCIE12_TXN/SATA2_TXN
		B25	PCIE12_TXP/SATA2_TXP

Pin	Signal	Pin	Signal	Net	Pin	Note
H8	USB3_1_RXN	USB30_RX_N1	29			Left USB3.0
G8	USB3_1_RXP	USB30_RX_P1	29			
C13	USB3_1_TXN	USB30_TX_N1	29			
D13	USB3_1_TXP	USB30_TX_P1	29			
J6	USB3_2_RXN/SSIC_1_RXN	USB30_RX_N2	33			Right USB3.0
H6	USB3_2_RXP/SSIC_1_RXP	USB30_RX_P2	33			
B13	USB3_2_TXN/SSIC_1_TXN	USB30_TX_N2	33			
A13	USB3_2_TXP/SSIC_1_TXP	USB30_TX_P2	33			
J10	USB3_3_RXN/SSIC_2_RXN					
H10	USB3_3_RXP/SSIC_2_RXP					
B15	USB3_3_TXN/SSIC_2_TXN					
A15	USB3_3_TXP/SSIC_2_TXP					
E10	USB3_4_RXN					
F10	USB3_4_RXP					
C15	USB3_4_TXN					
D15	USB3_4_TXP					
AB9	USB2N_1	USB20_N0	26			Camera_Conn
AB10	USB2P_1	USB20_P0	26			
AD6	USB2N_2	USB20_N1	33			Right USB2.0
AD7	USB2P_2	USB20_P1	33			
AH3	USB2N_3	USB20_N2	29			Left USB2.0
AJ3	USB2P_3	USB20_P2	29			
AD9	USB2N_4	USB20_N3	29			Card Reader
AD10	USB2P_4	USB20_P3	29			
AJ1	USB2N_5	USB20_N4	31			Mini Card BT
AJ2	USB2P_5	USB20_P4	31			
AF6	USB2N_6					EC T8396 Sensor
AF7	USB2P_6					
AH1	USB2N_7	USB20_N6	26			Touch Panel
AH2	USB2P_7	USB20_P6	26			
AF8	USB2N_8	USB20_N7	38			DC_IN combo USB2.0
AF9	USB2P_8	USB20_P7	38			
AG1	USB2N_9					
AG2	USB2P_9					
AH7	USB2N_10					
AH8	USB2P_10					
AB6	USB2_COMP	USB2_COMP	RC118 2	1 113_0402_1%		USBRBIAS
AG3	USB2_ID	USB2_ID	RC2535 2	1 0_0402_5%		Width 20Mil
AG4	USB2_VBUSSENSE	USB2_VBUSSENSE	RC2536 2	1 1K_0402_5%		Space 15Mil
						Length 500Mil
A9	GPP_E9/USB2_OC0#	USB_OC0#	33			
C9	GPP_E10/USB2_OC1#	USB_OC1#	29			
D9	GPP_E11/USB2_OC2#	USB_OC2#				
B9	GPP_E12/USB2_OC3#	USB_OC3#	38			
J1	GPP_E4/DEVSLP0	GPP_E4				
J2	GPP_E5/DEVSLP1					
J3	GPP_E6/DEVSLP2					
H2	GPP_E0/SATAXPCIE0/SATAGP0	SATA0GP				
H3	GPP_E1/SATAXPCIE1/SATAGP1	SATA1GP				
G4	GPP_E2/SATAXPCIE2/SATAGP2	SATA2GP				
H1	GPP_E8/SATALED#	BOARD_ID2			BOARD_ID2	7

SKYLAKE-U_BGA1356
REV = 1
@
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WLAN PCIE6

Pin	Signal	Pin	Signal	Net	Pin	Signal
31	PCIE_PRX_DTX_N6	PCIE_PRX_DTX_N6	G18	CC177 2	1 .1U_0402_10V6-K	PCIE_PRX_DTX_N6
31	PCIE_PRX_DTX_P6	PCIE_PRX_DTX_P6	F18	CC188 2	1 .1U_0402_10V6-K	PCIE_PRX_DTX_P6
31	PCIE_PTX_C_DRX_N6	PCIE_PTX_DRX_N6	D20			
31	PCIE_PTX_C_DRX_P6	PCIE_PTX_DRX_P6	C20			

Pin	Signal	Pin	Signal
33	SATA_PRX_DTX_N0	SATA_PRX_DTX_N0	F20
33	SATA_PRX_DTX_P0	SATA_PRX_DTX_P0	E20
33	SATA_PTX_DRX_N0	SATA_PTX_DRX_N0	B21
33	SATA_PTX_DRX_P0	SATA_PTX_DRX_P0	A21

third-part dGPU PCIEP9

Net	Pin	Signal	Pin	Signal
PCIE_CTX_C_GRX_N0	0.22U_0402_10V6K OPT@1	2 CC16	PCIE_CRX_GTX_N0	E22
PCIE_CTX_C_GRX_P0	0.22U_0402_10V6K OPT@1	2 CC14	PCIE_CRX_GTX_P0	E23
			PCIE_CTX_GRX_N0	B23
			PCIE_CTX_GRX_P0	A23
PCIE_CTX_C_GRX_N1	0.22U_0402_10V6K OPT@1	2 CC15	PCIE_CRX_GTX_N1	F25
PCIE_CTX_C_GRX_P1	0.22U_0402_10V6K OPT@1	2 CC17	PCIE_CRX_GTX_P1	E25
			PCIE_CTX_GRX_N1	D23
			PCIE_CTX_GRX_P1	C23
RC119 1	2 100_0402_1%		PCIE_RCOMPN	F5
			PCIE_RCOMPP	E5
PAD @ TP20	1		XDP_PRDY#	D56
PAD @ TP19	1		XDP_PREQ#	D61
			PIRQA#	BB11
PCIE_CTX_C_GRX_N2	0.22U_0402_10V6K OPT@1	2 CC18	PCIE_CRX_GTX_N2	E28
PCIE_CTX_C_GRX_P2	0.22U_0402_10V6K OPT@1	2 CC19	PCIE_CRX_GTX_P2	E27
			PCIE_CTX_GRX_N2	D24
			PCIE_CTX_GRX_P2	C24
			PCIE_CRX_GTX_N3	E30
			PCIE_CRX_GTX_P3	F30
PCIE_CTX_C_GRX_N3	0.22U_0402_10V6K OPT@1	2 CC20	PCIE_CTX_GRX_N3	A25
PCIE_CTX_C_GRX_P3	0.22U_0402_10V6K OPT@1	2 CC21	PCIE_CTX_GRX_P3	B25

PCIE_RCOMPN and PCIE_RCOMPP
Trace Width: 12-15mil
Differential between RCOMPP/RCOMPN

Pin	Signal
18	PCIE_CRX_GTX_N[0..3]
18	PCIE_CRX_GTX_P[0..3]
18	PCIE_CTX_C_GRX_N[0..3]
18	PCIE_CTX_C_GRX_P[0..3]

+3VS

RPC2 — 10K_0804_8P4R_5%

Pin	Signal	Pin	Signal
1		8	SATA1GP
2		7	SATA0GP
3		6	SATA2GP
4		5	PIRQA#

+3VALW_PCH

RPC17 — 10K_0804_8P4R_5%

Pin	Signal	Pin	Signal
8	USB_OC0#	1	
7	USB_OC1#	2	
6	USB_OC3#	3	
5	USB_OC2#	4	

+3VS

GPP_E4 RC1617 2 — @ — 1 10K_0402_5%

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Title: MCP (PCIE,SATA,USB3,US

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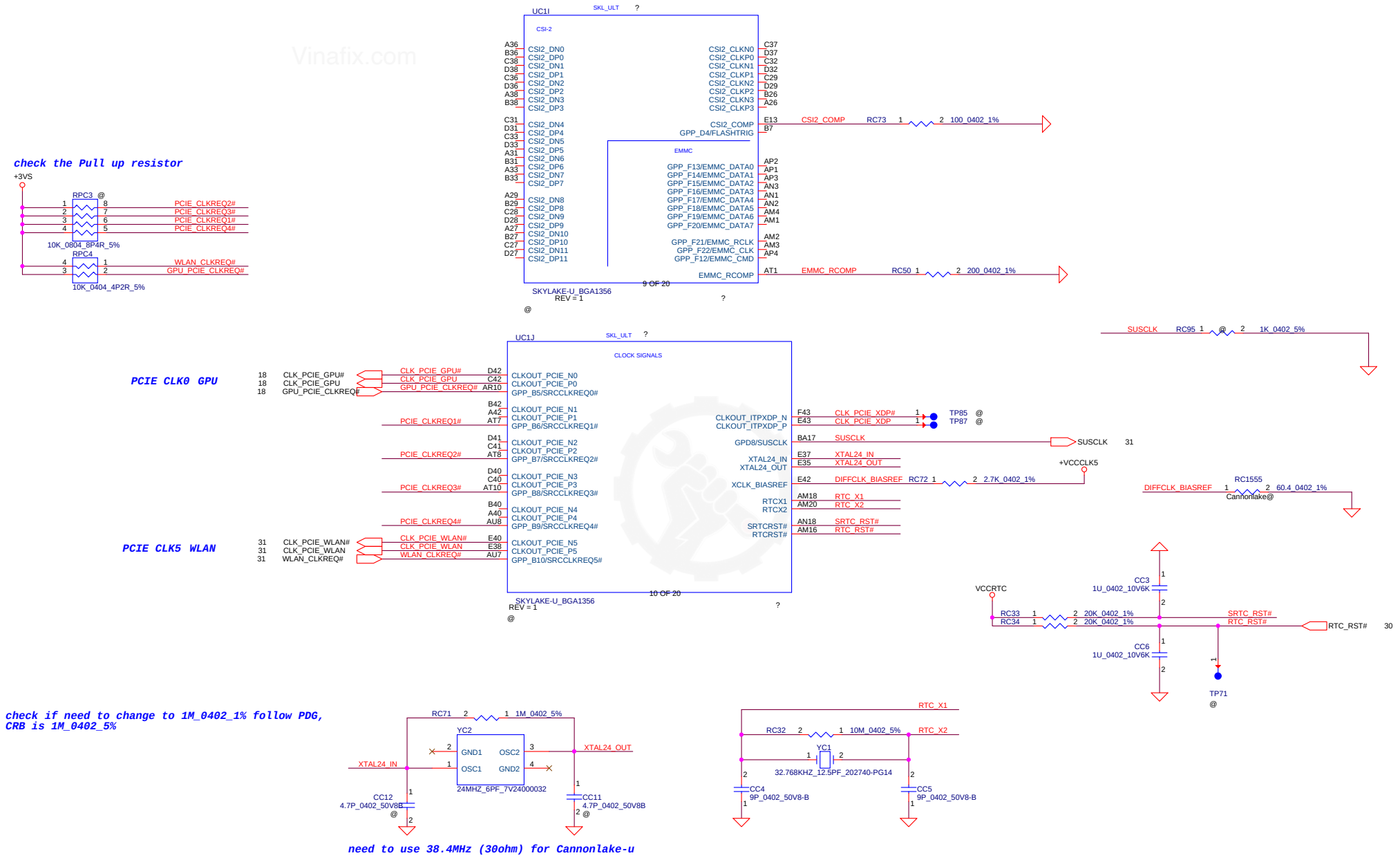
Date: Wednesday, July 22, 2015 | Sheet 8 of 46



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Title: MCP (CSI2,EMMC,CLOCK)

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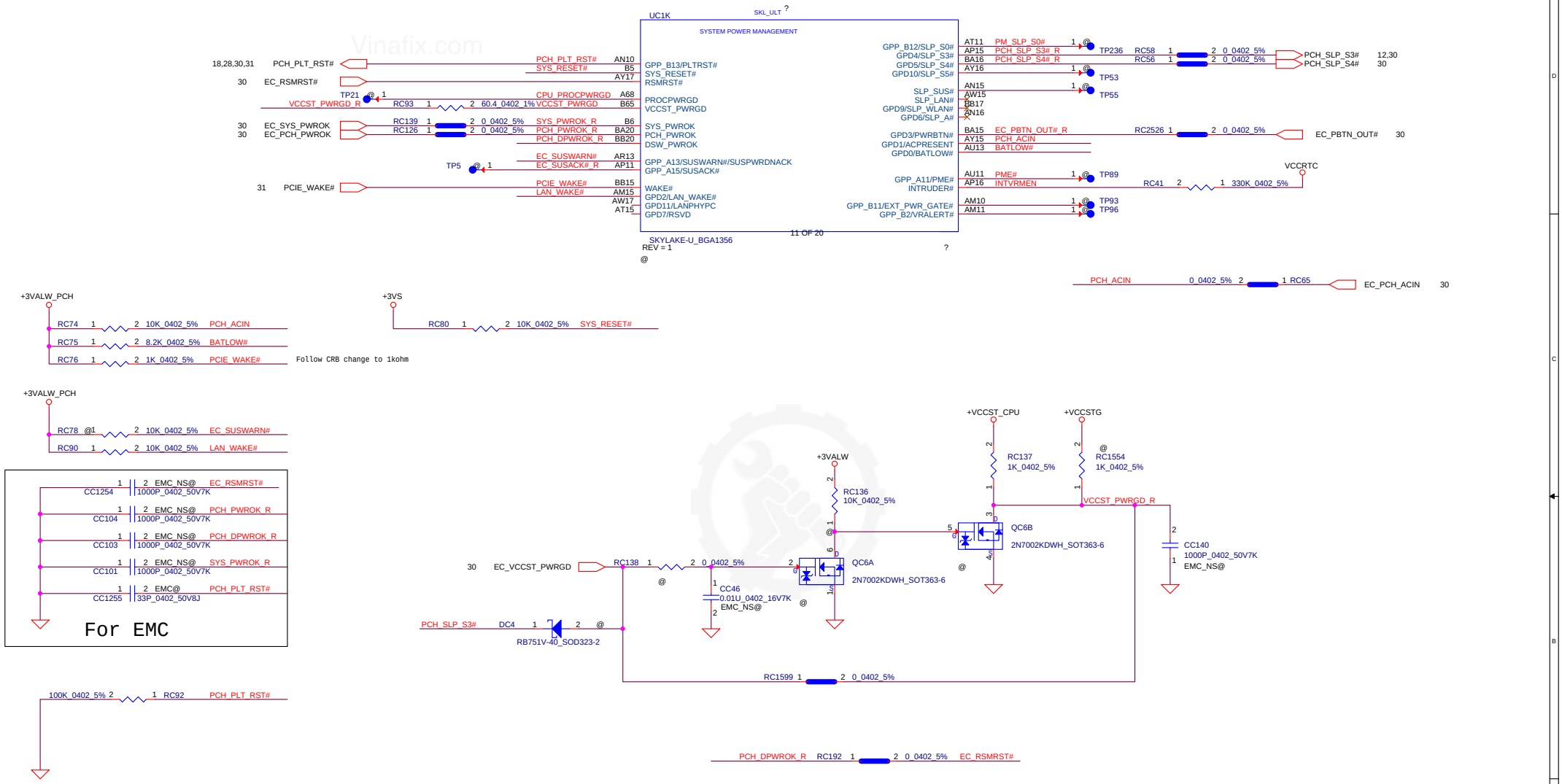

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Title: MCP (SYSTEM PWR MANAGEMENT)

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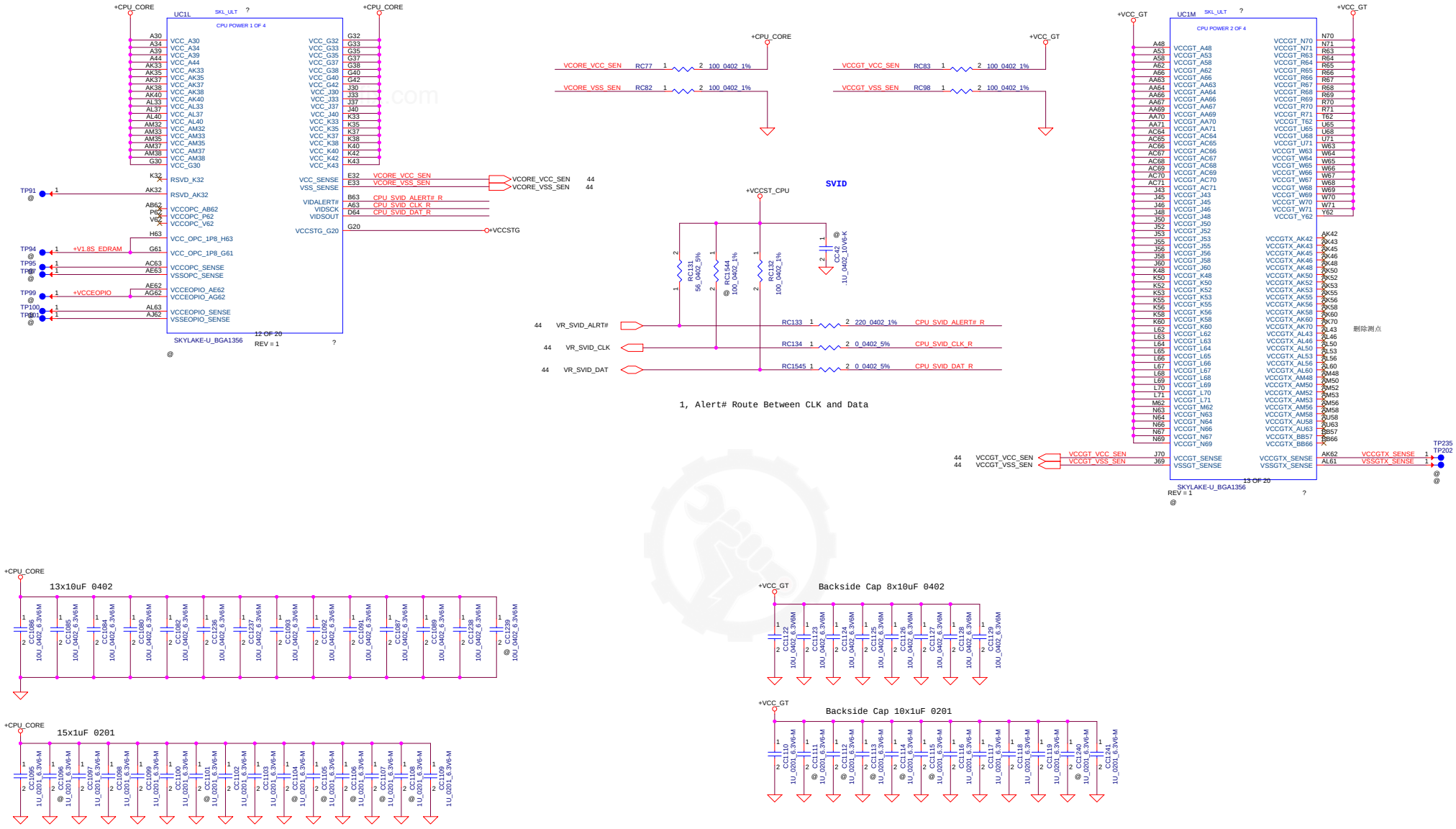
Date: Wednesday, July 22, 2015 | Sheet 10 of 46



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Title: **MCP (CPU PWR1)**

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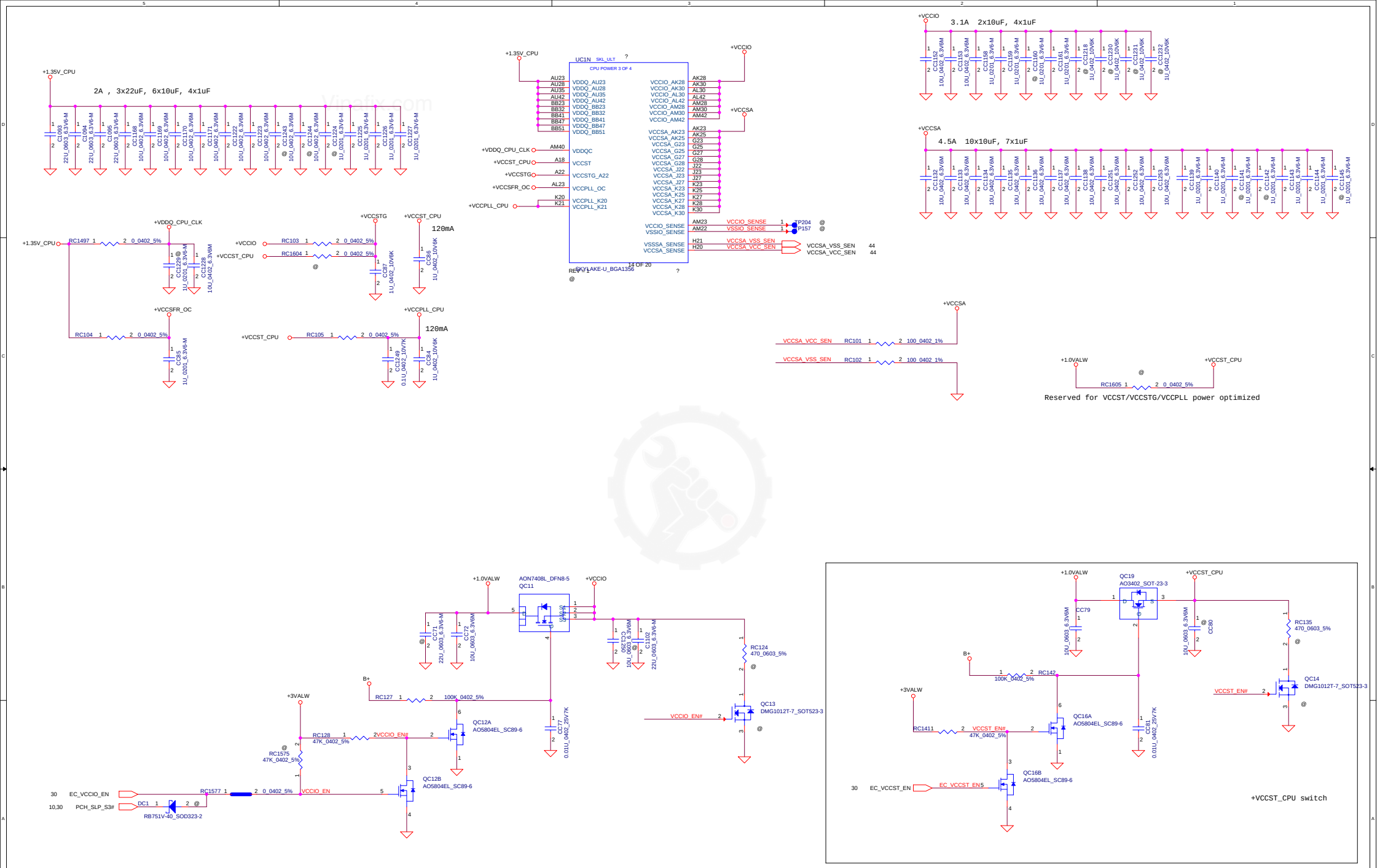

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Title: **MCP (CPU PWR2)**

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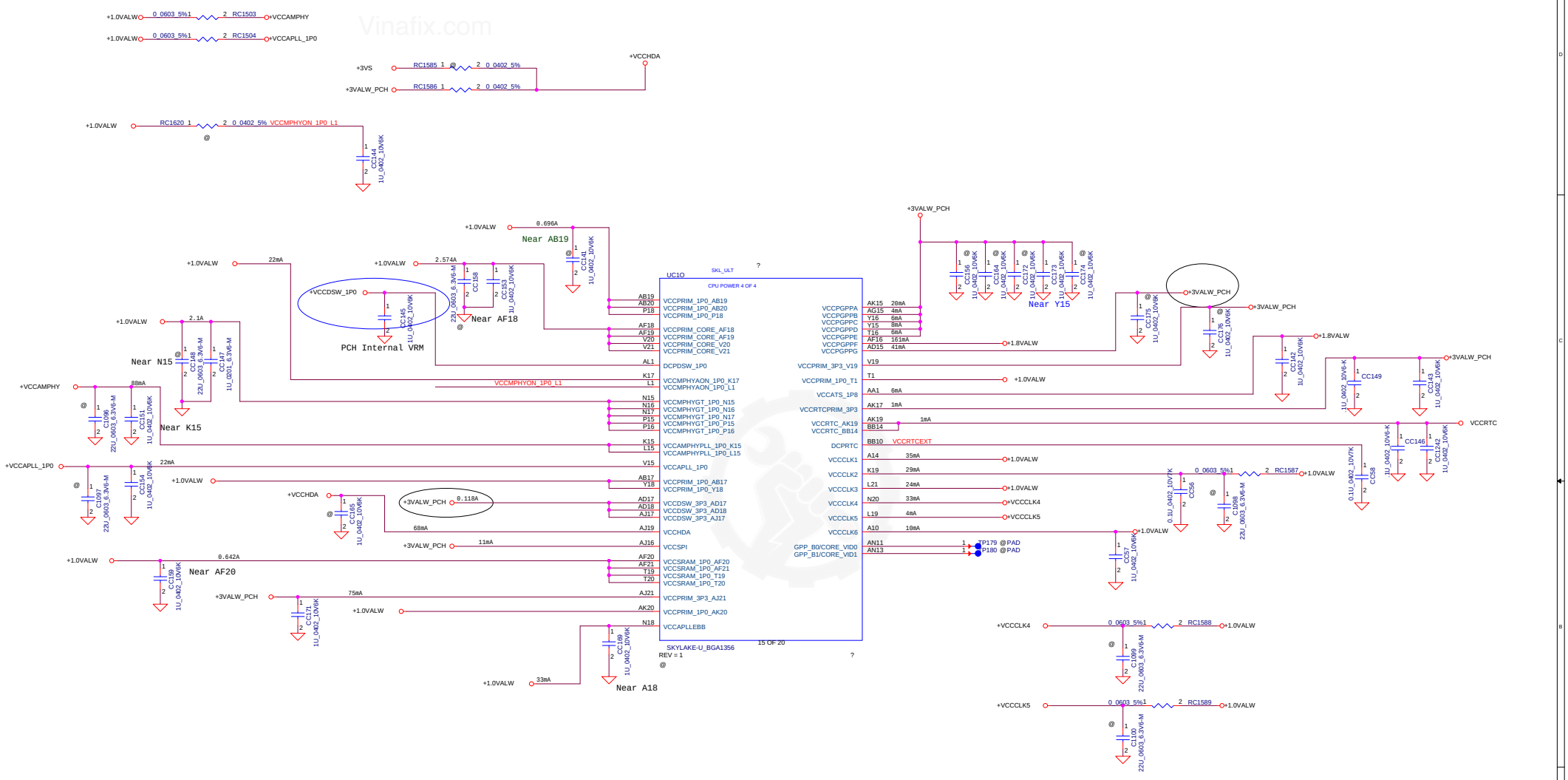

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Title: **MCP (PCH PWR)**

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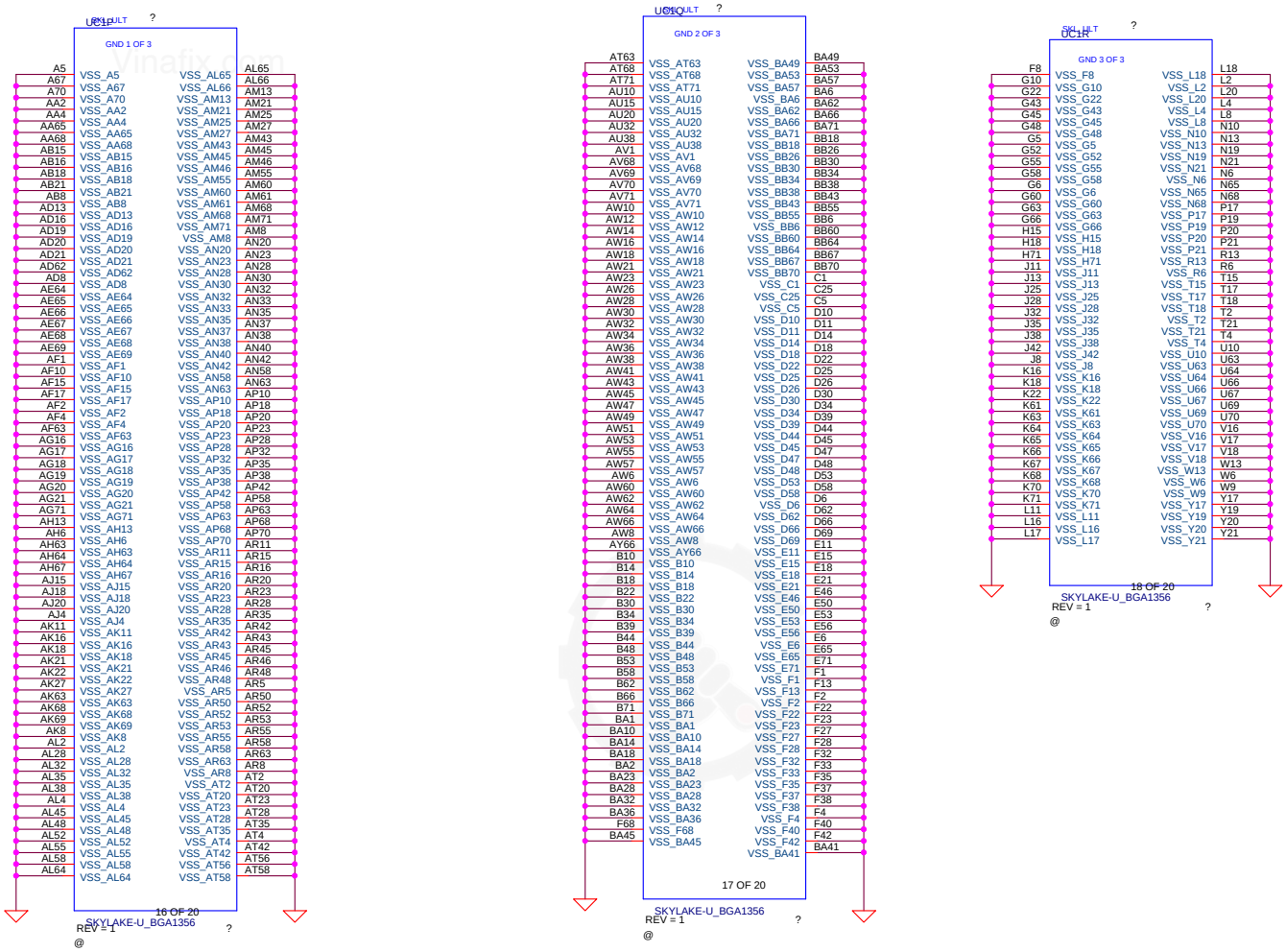

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Title: **MCP (VSS)**

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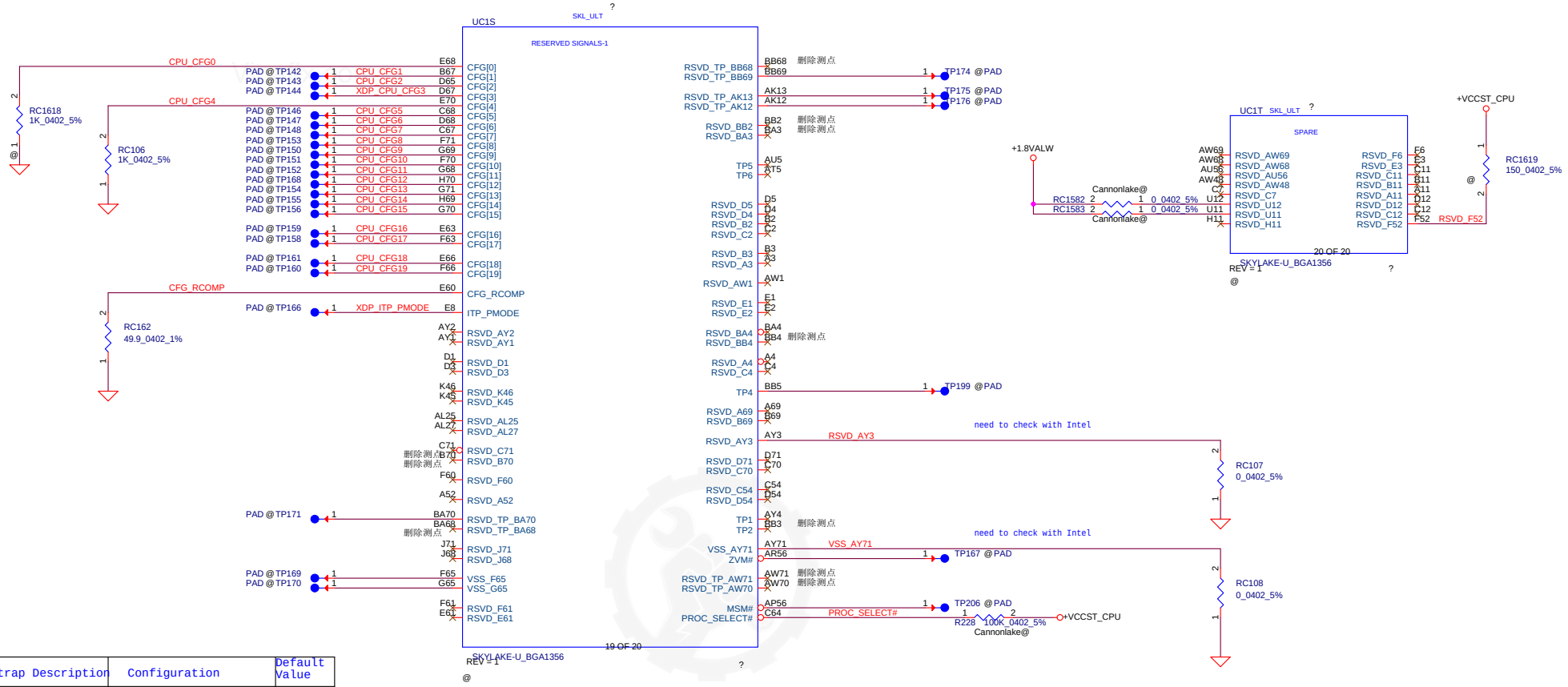

Pin Name	Strap Description	Configuration	Default Value
CFG[4]	Display Port Presence strap	–1 = eDP Disabled –0 = eDP Enabled *	1

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Title: **MCP (CFG,RESERVED)**

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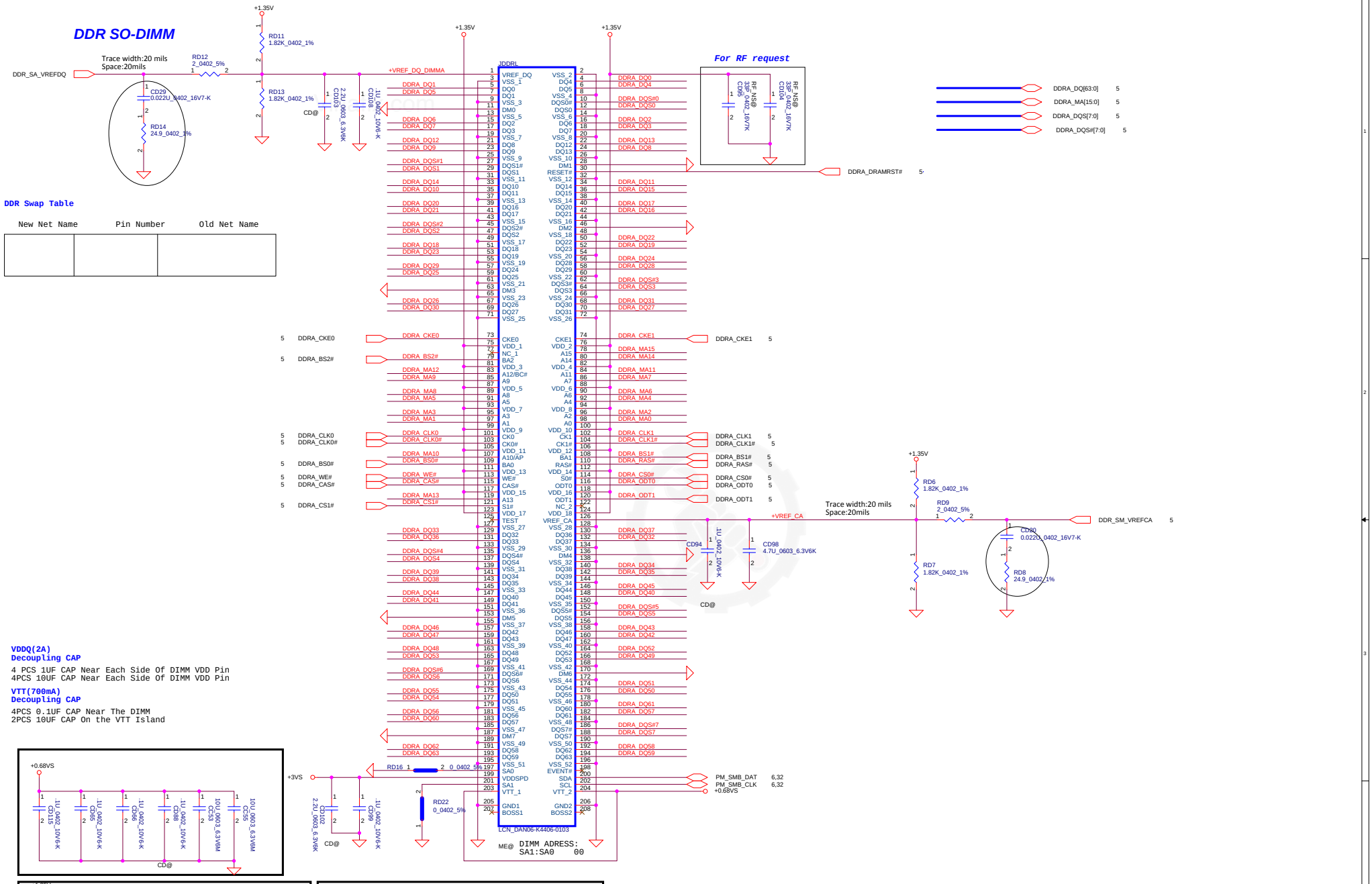
DDR SO-DIMM



DDR Swap Table

New Net Name	Pin Number	Old Net Name

VDDQ(2A)
Decoupling CAP

4 PCS 1UF CAP Near Each Side Of DIMM VDD Pin
4PCS 10UF CAP Near Each Side Of DIMM VDD Pin

VTT(700mA)
Decoupling CAP

4PCS 0.1UF CAP Near The DIMM
2PCS 10UF CAP On the VTT Island

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Title: DDR3L

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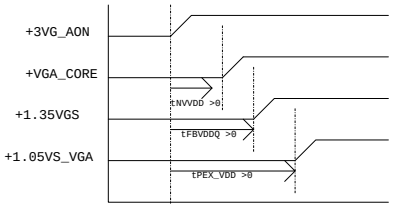
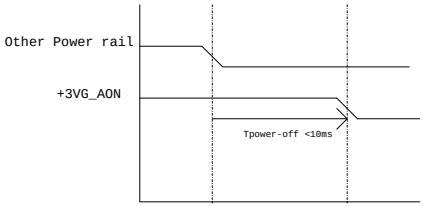
N15x GPIO

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	FB Enable for GC6 2.0
GPIO1	OUT	N/A	
GPIO2	OUT	N/A	
GPIO3	OUT	N/A	
GPIO4	OUT	N/A	
GPIO5	OUT	N/A	GPU power sequencing---3V3_MAIN_EN
GPIO6	IN	-	GPU wake signal for GC6 2.0
GPIO7	OUT	N/A	
GPIO8	I/O	-	System side PCIe reset Monitor
GPIO9	I/O	N/A	2.2K Pull-up
GPIO10	OUT	N/A	
GPIO11	OUT	-	GPU Core VDD PWM control signal
GPIO12	IN		AC Power Detect Input (10K pull High)
GPIO13	OUT	-	Phase Shedding
GPIO14	IN	N/A	
GPIO15	IN	N/A	
GPIO16		N/A	
GPIO17	IN	N/A	
GPIO18	IN	N/A	
GPIO19	IN	N/A	
GPIO20		N/A	
GPIO21	OUT		GPU PCIe self-reset control
OVERT	OUT		Active Low Thermal Catastrophic Over Temperature

N15V-GM Power Sequence

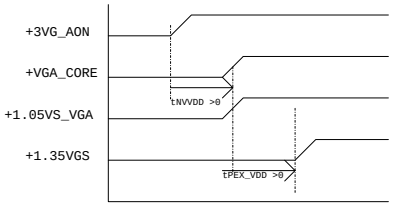


1. all power rail ramp up time should be larger than 40us



1.all GPU power rails should be turned off within 10ms
2. Optimus system VDD33 avoids drop down earlier than NVDD and FBVDDQ

N15S-GT Power Sequence



1. all power rail ramp up time should be larger than 40us and less than 2ms .

Performance Mode P0 TDP at Tj = 102 C* (DDR3)

Products	GPU (4) (W)	Mem (1,5) (W)	NVCLK /MCLK (MHz)	NVVDD (V)	NVVDD (A)	NVVDD (W)	FBVDD (1.35V) (A)	FBVDD (1.35V) (W)	FBVDDQ (GPU+Mem) (1.35V) (A)	FBVDDQ (GPU+Mem) (1.35V) (W)	PCI Express (1.05V) (6) (mA)	PCI Express (1.05V) (6) (W)		I/O and PLLVDD (1.05V) (mA)	I/O and PLLVDD (1.05V) (W)	Other (3.3V) (mA)	Other (3.3V) (W)
N14X 128bit 2GB DDR3	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD		TBD	TBD	TBD	TBD

N15x Multi-level Straps

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VGS	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	+3VGS	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VGS	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VGS	Reserved(keep pull-up and pull-down footprint and stuff 50Kohm pull-up)			
STRAP1	+3VGS	Reserved(keep pull-up and pull-down footprint and not stuff by default)			
STRAP2	+3VGS				
STRAP3	+3VGS				
STRAP4	+3VGS				

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

N15x Binary Straps

Physical Strapping pin	Power Rail	Strap Mapping
ROM_SCLK	+3VGS	SMB_ALT_ADDR
ROM_SI	+3VGS	SUB_VENDOR
ROM_SO	+3VGS	VGA_DEVICE
STRAP0	+3VGS	RAM_CFG[0]
STRAP1	+3VGS	RAM_CFG[1]
STRAP2	+3VGS	RAM_CFG[2]
STRAP3	+3VGS	RAM_CFG[3]
STRAP4	+3VGS	PCIE_MAX_SPEED

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Title: VGA Notes List

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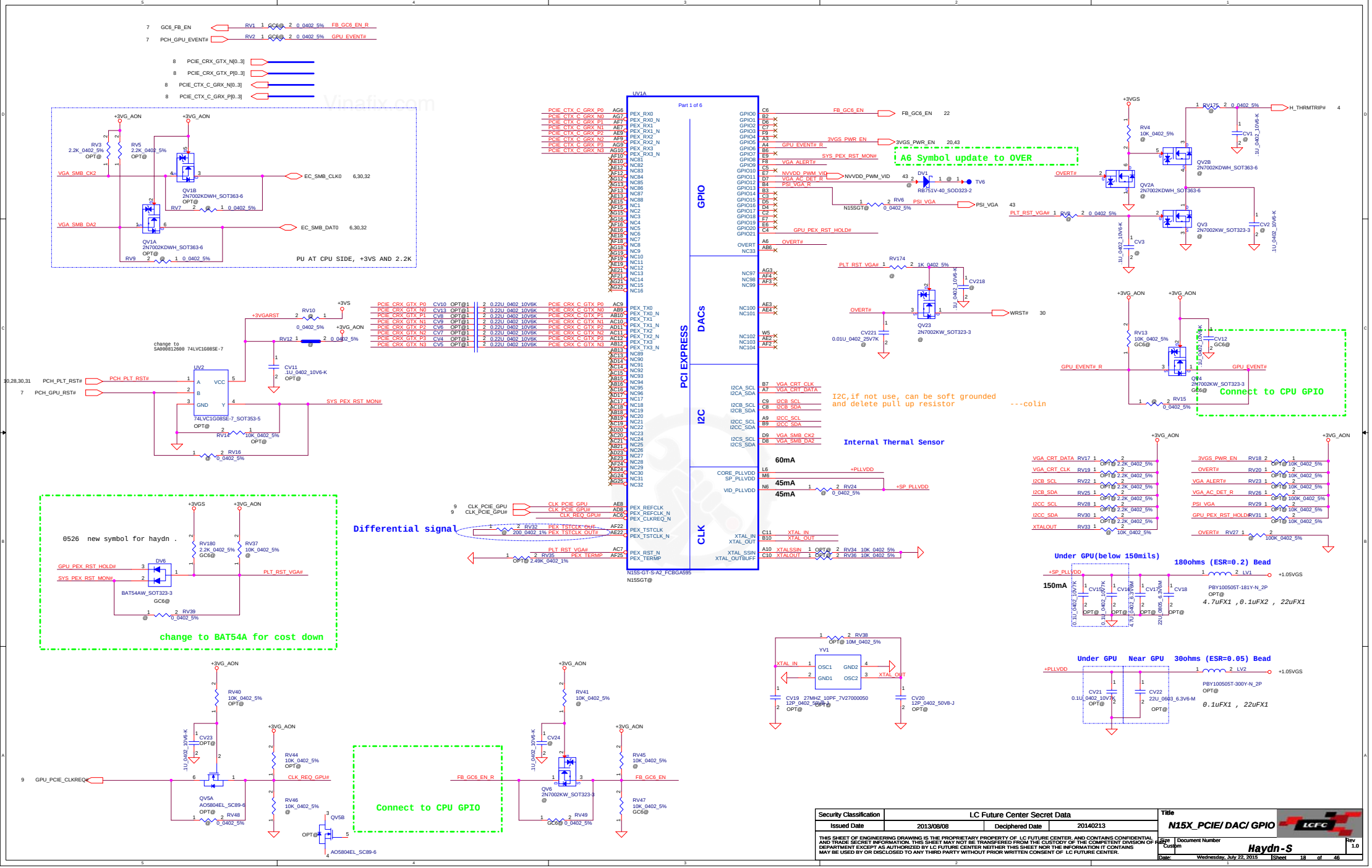
UV1A
Part 1 of 6
PCI EXPRESS
GPIO
DACs
I2C
CLK
N15S-GT-S-A2_FCBGA595
N15SGT@
PU AT CPU SIDE, +3VS AND 2.2K
A6 Symbol update to OVER
Connect to CPU GPIO
I2C,if not use, can be soft grounded and delete pull up resistor ---colin
Internal Thermal Sensor
Differential signal
0526 new symbol for haydn .
change to BAT54A for cost down
Under GPU(below 150mils)
180ohms (ESR=0.2) Bead
150mA
4.7uFX1 ,0.1uFX2 , 22uFX1
Under GPU Near GPU 30ohms (ESR=0.05) Bead
0.1uFX1 , 22uFX1
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2013/08/08
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Title
N15X_PCIE/ DAC/ GPIO
Size
Custom
Document Number
Haydn-S
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1.0
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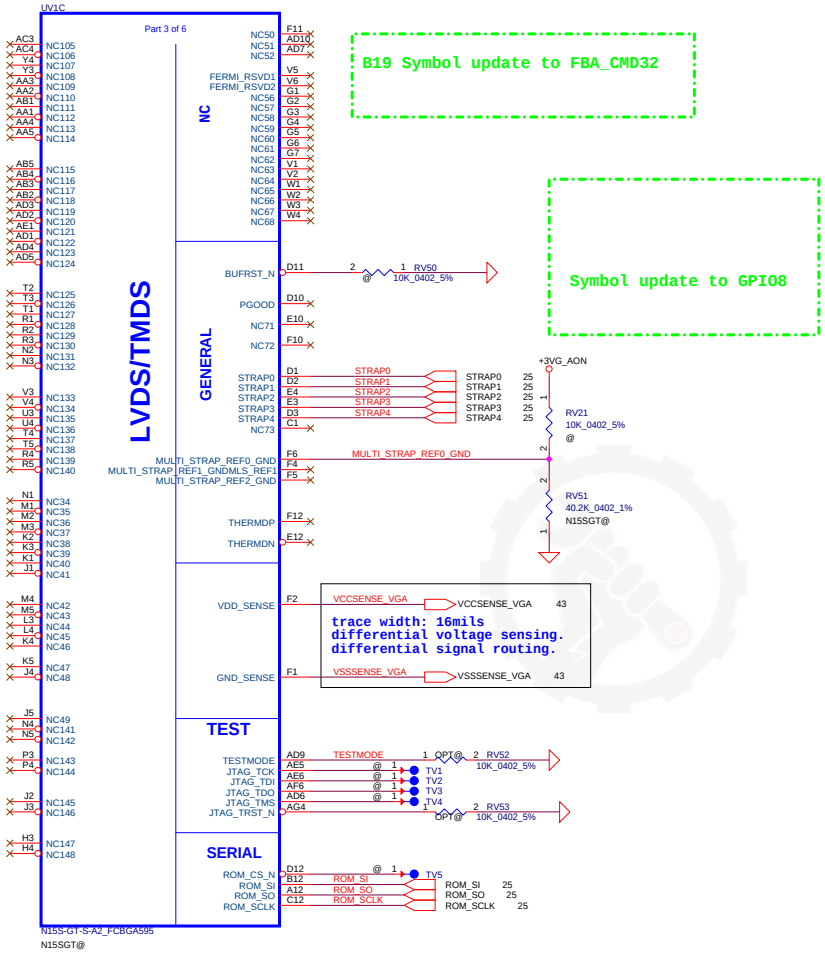

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Title: N15X_LVDS/ HDMI/ THERM

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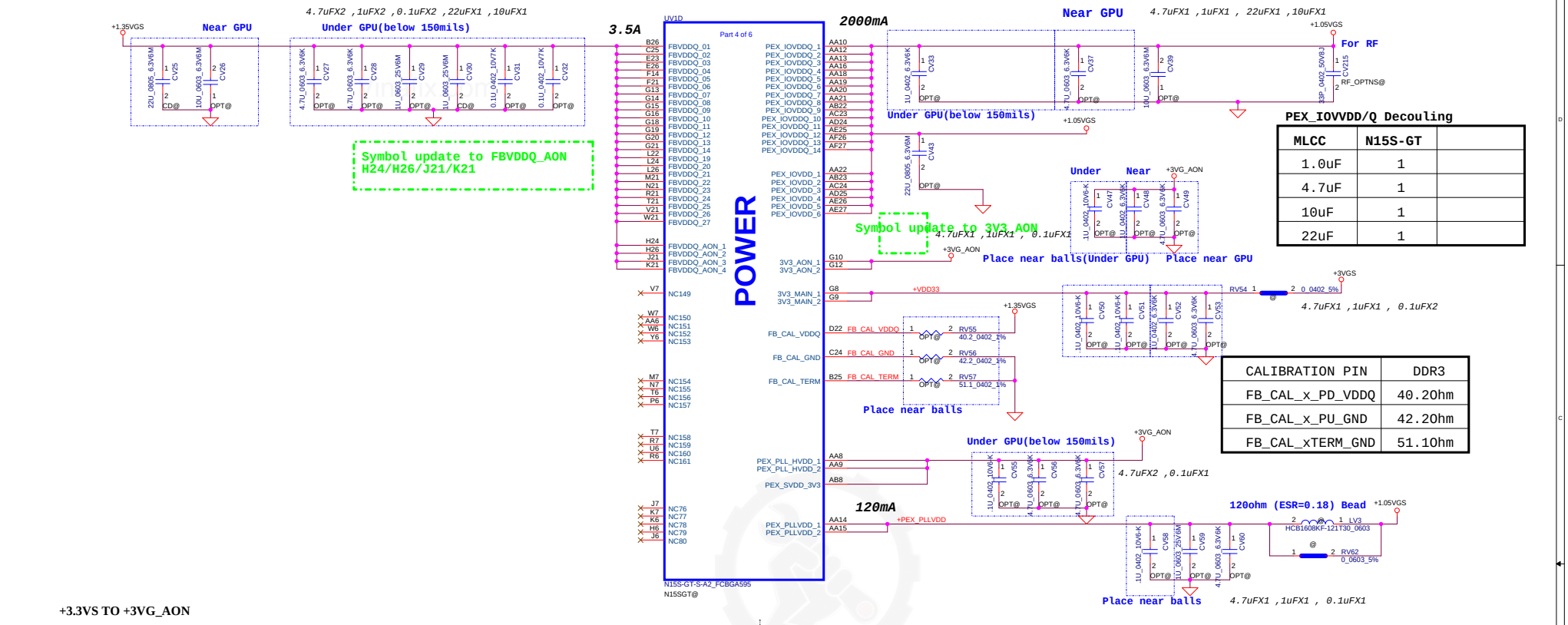
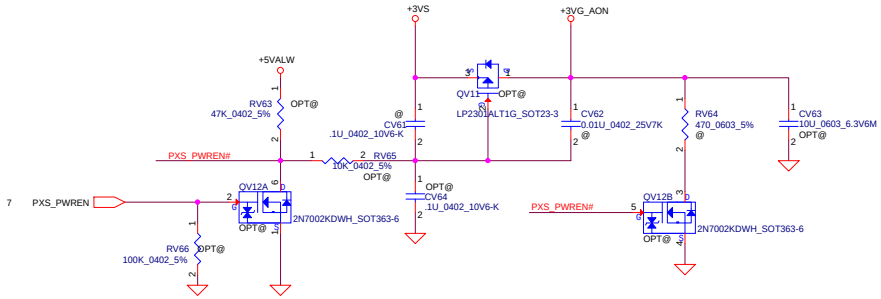


PEX_IOVVDD/Q Decouling

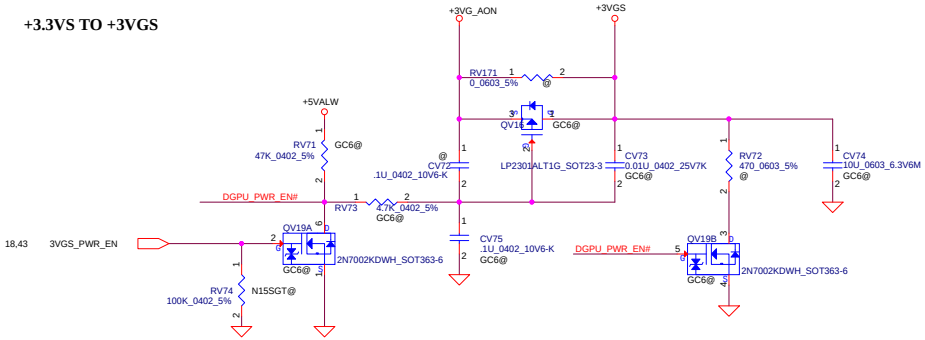
MLCC	N15S-GT	
1.0uF	1	
4.7uF	1	
10uF	1	
22uF	1	

CALIBRATION PIN	DDR3
FB_CAL_x_PD_VDDQ	40.2Ohm
FB_CAL_x_PU_GND	42.2Ohm
FB_CAL_xTERM_GND	51.1Ohm

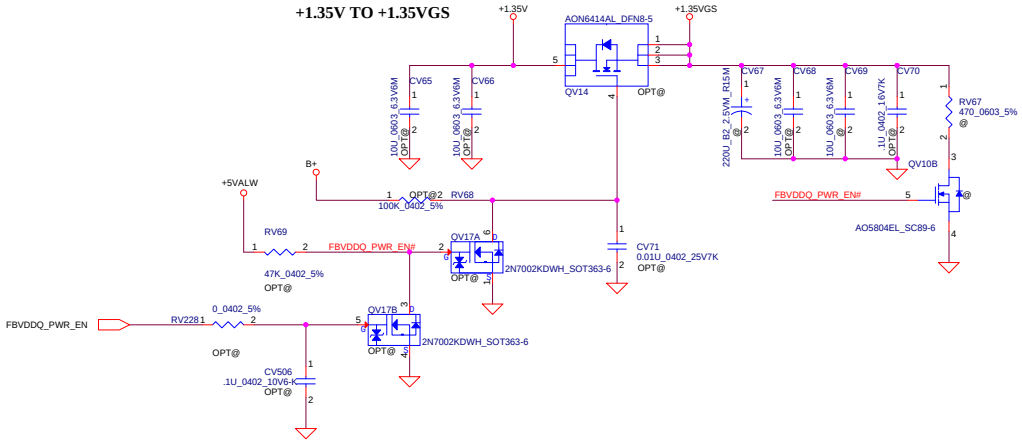
+3.3VS TO +3VG_AON



+3.3VS TO +3VGS



+1.35V TO +1.35VGS



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Title: **N15X_Power**

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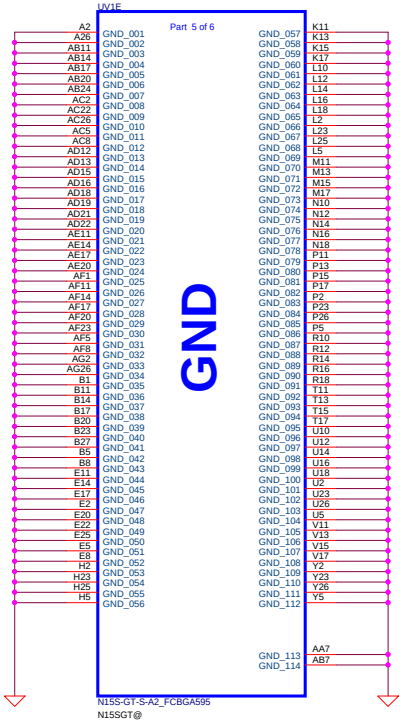

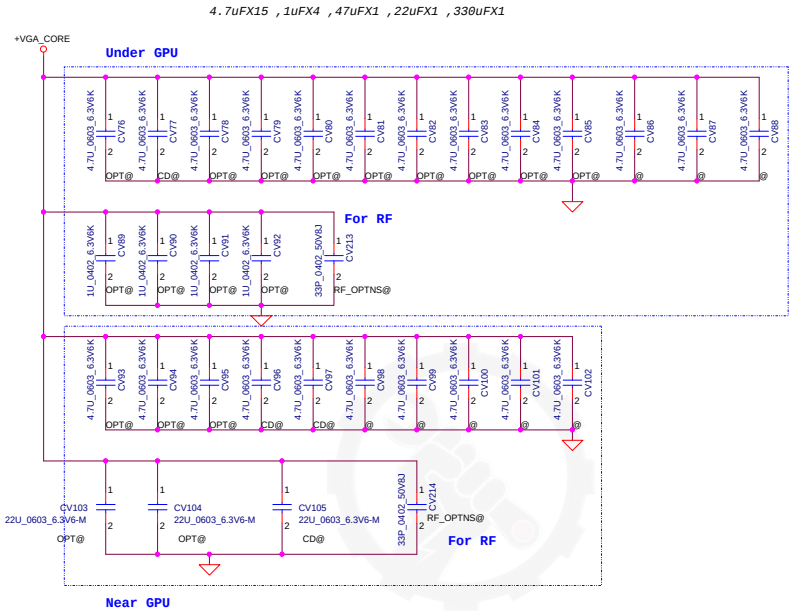

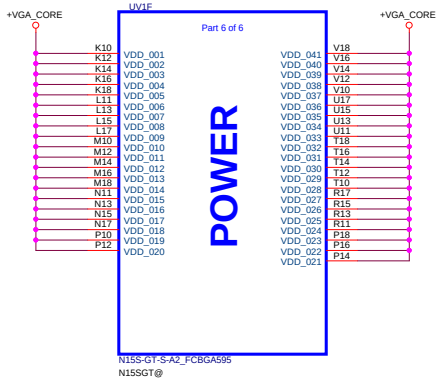

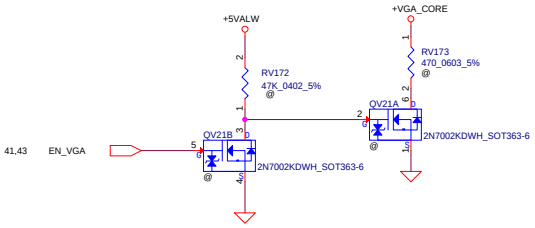

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Title: N15X_+VGA CORE, GND

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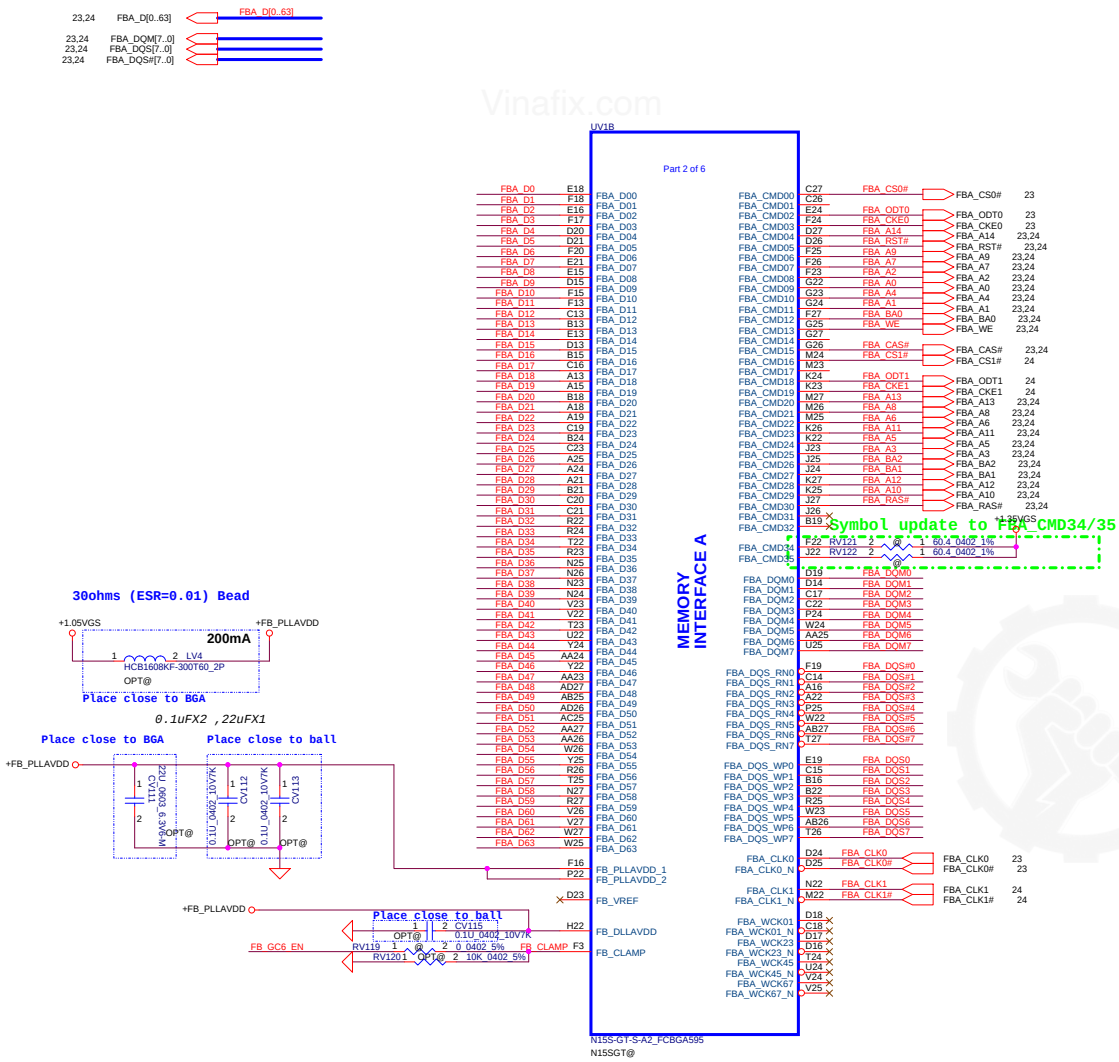

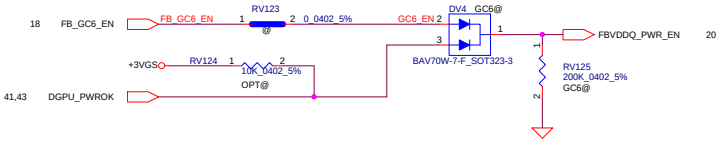

CMD mapping mod Mode D

	Rank0			
Address	0..31	32..63		
FBx_CMD0	CS0#			
FBx_CMD1				
FBx_CMD2	ODT0			
FBx_CMD3	CKE0			
FBx_CMD4	A14	A14		
FBx_CMD5	RST	RST		
FBx_CMD6	A9	A9		
FBx_CMD7	A7	A7		
FBx_CMD8	A2	A2		
FBx_CMD9	A0	A0		
FBx_CMD10	A4	A4		
FBx_CMD11	A1	A1		
FBx_CMD12	BA0	BA0		
FBx_CMD13	WE	WE		
FBx_CMD14	A15	A15		
FBx_CMD15	CAS#	CAS#		
FBx_CMD16		CS1#		
FBx_CMD17				
FBx_CMD18		ODT1		
FBx_CMD19		CKE1		
FBx_CMD20	A13	A13		
FBx_CMD21	A8	A8		
FBx_CMD22	A6	A6		
FBx_CMD23	A11	A11		
FBx_CMD24	A5	A5		
FBx_CMD25	A3	A3		
FBx_CMD26	BA2	BA2		
FBx_CMD27	BA1	BA1		
FBx_CMD28	A12	A12		
FBx_CMD29	A10	A10		
FBx_CMD30	RAS#	RAS#		
FBx_CMD31				
FBx_CMD32				
FBx_CMD33				
FBx_CMD34	DBG0			
FBx_CMD35	DBG1			

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Title: **N15X_MEM Interface**

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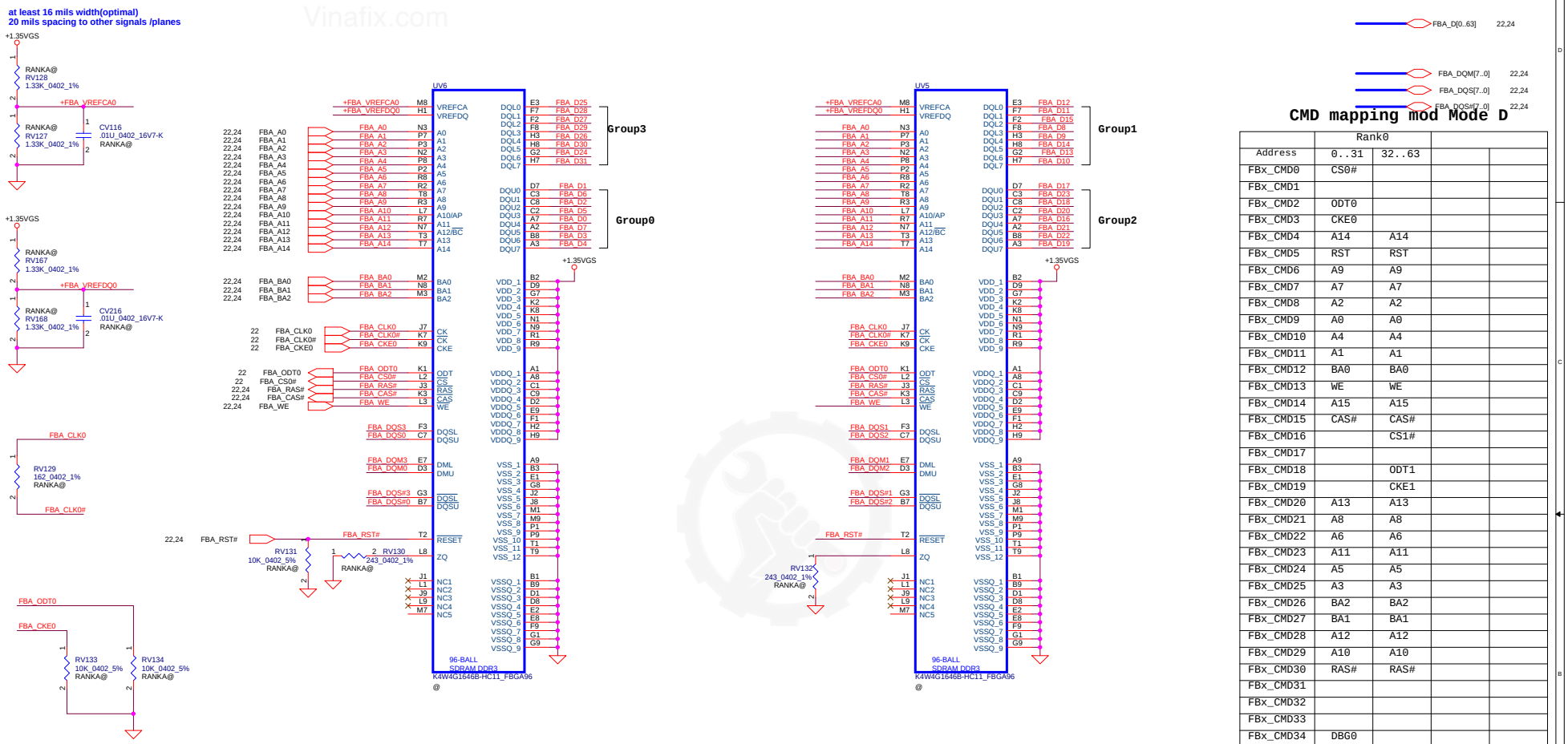
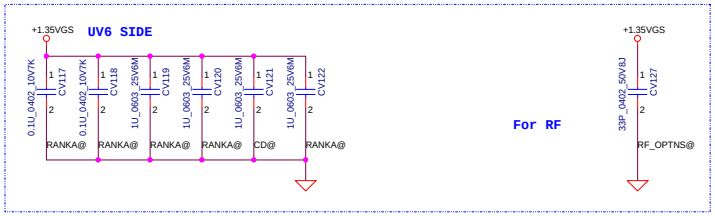
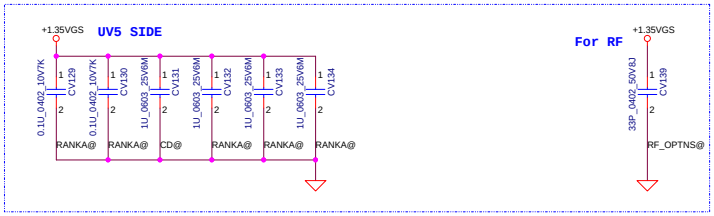
Vinafix.com



CMD mapping mod Mode D

	Rank0			
Address	0..31	32..63		
FBx_CMD0	CS0#			
FBx_CMD1				
FBx_CMD2	ODT0			
FBx_CMD3	CKE0			
FBx_CMD4	A14	A14		
FBx_CMD5	RST	RST		
FBx_CMD6	A9	A9		
FBx_CMD7	A7	A7		
FBx_CMD8	A2	A2		
FBx_CMD9	A0	A0		
FBx_CMD10	A4	A4		
FBx_CMD11	A1	A1		
FBx_CMD12	BA0	BA0		
FBx_CMD13	WE	WE		
FBx_CMD14	A15	A15		
FBx_CMD15	CAS#	CAS#		
FBx_CMD16		CS1#		
FBx_CMD17				
FBx_CMD18		ODT1		
FBx_CMD19		CKE1		
FBx_CMD20	A13	A13		
FBx_CMD21	A8	A8		
FBx_CMD22	A6	A6		
FBx_CMD23	A11	A11		
FBx_CMD24	A5	A5		
FBx_CMD25	A3	A3		
FBx_CMD26	BA2	BA2		
FBx_CMD27	BA1	BA1		
FBx_CMD28	A12	A12		
FBx_CMD29	A10	A10		
FBx_CMD30	RAS#	RAS#		
FBx_CMD31				
FBx_CMD32				
FBx_CMD33				
FBx_CMD34	DBG0			
FBx_CMD35	DBG1			





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Title: **DDR3 VRAM Rank0_L**

Size: C | Document Number: **Haydn-S** | Rev: 1.0

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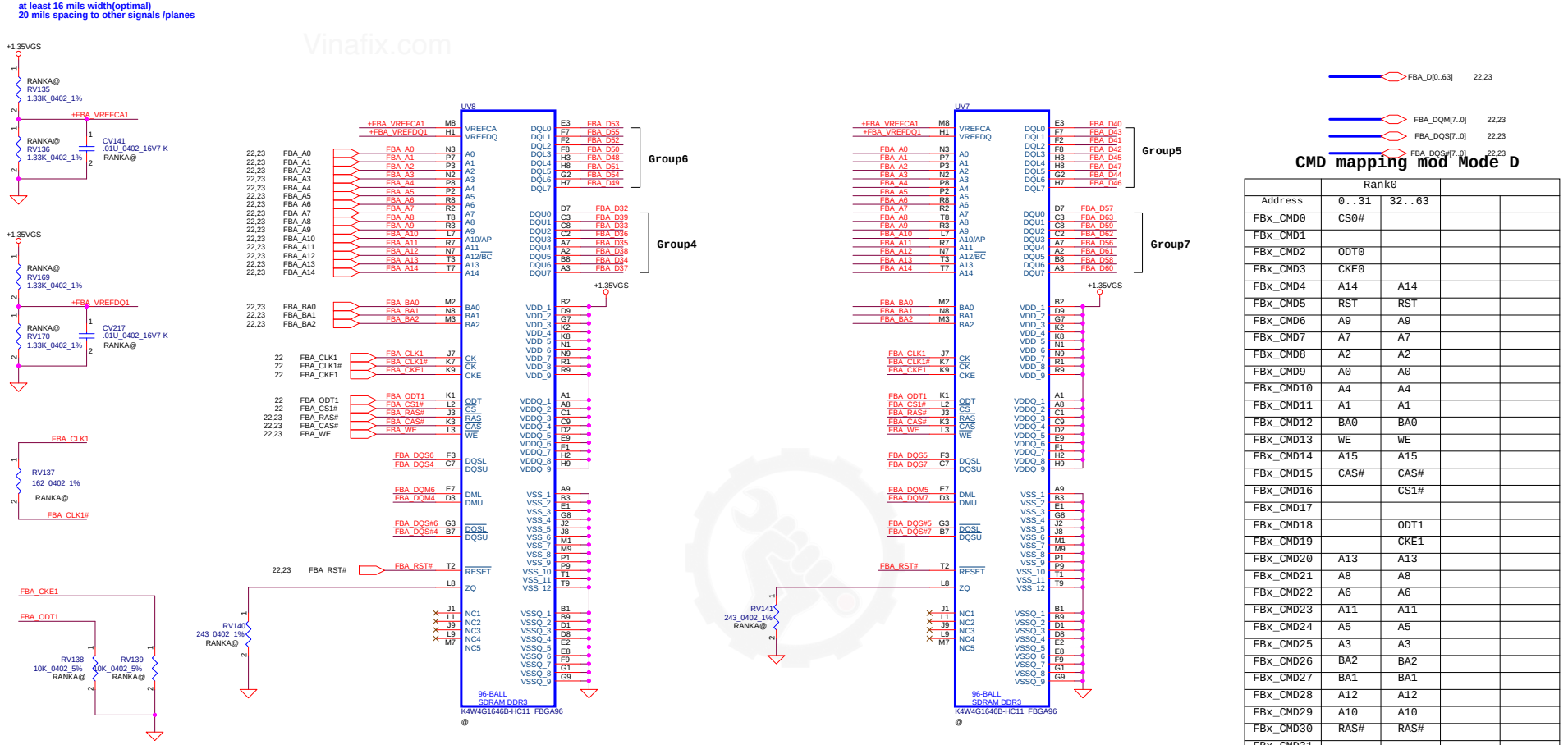
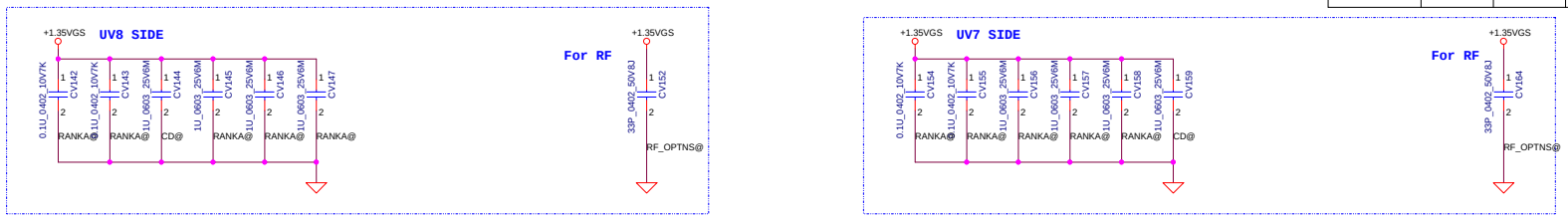


CMD mapping mod Mode D

	Rank0			
Address	0..31	32..63		
FBx_CMD0	CS0#			
FBx_CMD1				
FBx_CMD2	ODT0			
FBx_CMD3	CKE0			
FBx_CMD4	A14	A14		
FBx_CMD5	RST	RST		
FBx_CMD6	A9	A9		
FBx_CMD7	A7	A7		
FBx_CMD8	A2	A2		
FBx_CMD9	A0	A0		
FBx_CMD10	A4	A4		
FBx_CMD11	A1	A1		
FBx_CMD12	BA0	BA0		
FBx_CMD13	WE	WE		
FBx_CMD14	A15	A15		
FBx_CMD15	CAS#	CAS#		
FBx_CMD16		CS1#		
FBx_CMD17				
FBx_CMD18		ODT1		
FBx_CMD19		CKE1		
FBx_CMD20	A13	A13		
FBx_CMD21	A8	A8		
FBx_CMD22	A6	A6		
FBx_CMD23	A11	A11		
FBx_CMD24	A5	A5		
FBx_CMD25	A3	A3		
FBx_CMD26	BA2	BA2		
FBx_CMD27	BA1	BA1		
FBx_CMD28	A12	A12		
FBx_CMD29	A10	A10		
FBx_CMD30	RAS#	RAS#		
FBx_CMD31				
FBx_CMD32				
FBx_CMD33				
FBx_CMD34	DBG0			
FBx_CMD35	DBG1			



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Title: DDR3 VRAM Rank0_H

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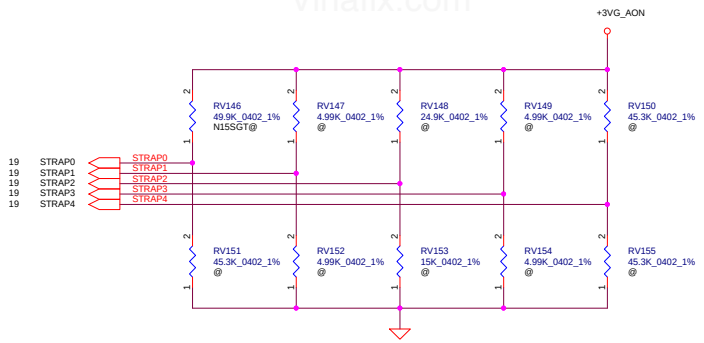
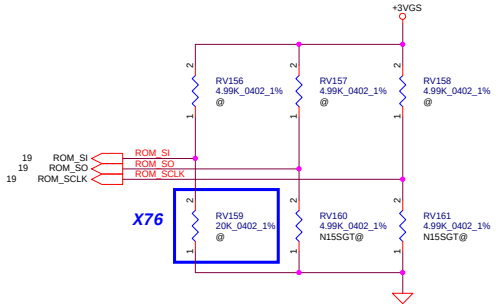




Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VGS	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	+3VGS	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VGS	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VGS	Reserved(keep pull-up and pull-down footprint and stuff 50Kohm pull-up)			
STRAP1	+3VGS	Reserved(keep pull-up and pull-down footprint and not stuff by default)			
STRAP2	+3VGS				
STRAP3	+3VGS				
STRAP4	+3VGS				

Resistor Values	Pull-up to +3VGS	Pull-down to Gnd
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

N15x Binary Straps

Physical Strapping pin	Power Rail	Strap Mapping
ROM_SCLK	+3VGS	SMB_ALT_ADDR
ROM_SI	+3VGS	SUB_VENDOR
ROM_SO	+3VGS	VGA_DEVICE
STRAP0	+3VGS	RAM_CFG[0]
STRAP1	+3VGS	RAM_CFG[1]
STRAP2	+3VGS	RAM_CFG[2]
STRAP3	+3VGS	RAM_CFG[3]
STRAP4	+3VGS	PCIE_MAX_SPEED

DEVID_SEL	
0	(Default)
1	

PCIE_CFG	
0	(Default)
1	

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

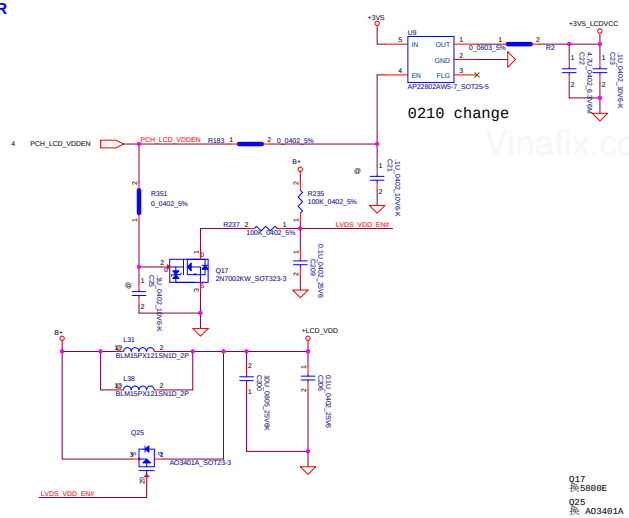
VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

X76

GPU	FB Memory (DDR3)		ROM_SI	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N16S-GT	Hynix 900MHz	H5TC4G63CFR-N0C	0x2	PD 4.99K	PD 4.99K	PU 49.9K	Un-stuff	Un-stuff	Un-stuff	Un-stuff
		256M x 16	PD 15K							
	Micron 900MHz	MT41J256M16HA-093G:E	0x4							
		256M x 16	PD 24.9K							
	Samsung 900MHz	K4W4G1646E-BC1A	0x1							
		256M x 16	PD 10K							
	Hynix 900MHz	H5TC2G63FFR-11C	0x9							
		128M x 16	PU 10K							
	Micron 900MHz	MT41J128M16JT-093G:K	0xA							
		128M x 16	PU 15K							
	Samsung 900MHz	K4W2G1646Q-BC1A	0xB							
		128M x 16	PU 20K							

VRAM	X76	VRAM P/N
Samsung	X7607312002	SA000063F20
Micron	X7607312003	SA000060I10
Hynix	X7607312001	SA00007DU10

LCD PWR



Q17
換5800E

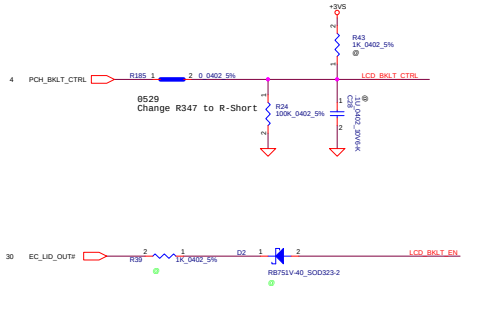
Q25
換 AO3401A

Hot-Plug

EDP_HPD

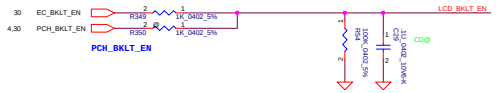
*EDP EN,EDP-HPD EN
EDP EN, EDP-HPD Disabled, 10K PU Via VCCIO
EDP Disabled, NC

BKLT CNTL



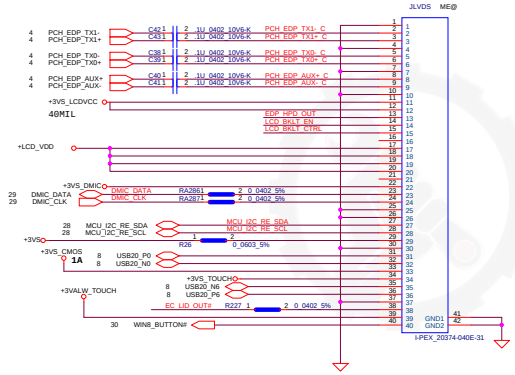
0529
Change R347 to R-Short

LCD背光控制，LID控制以及PCH的热键控制都NC，直接由EC来做背光控制.

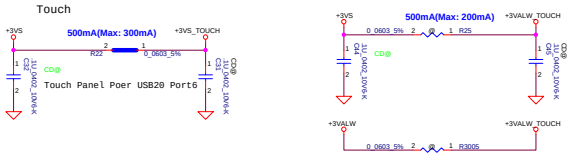


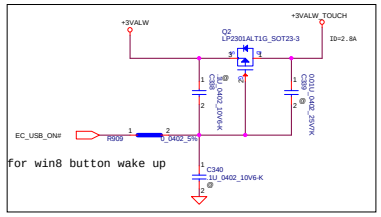
PCH_BKLT_EN

For LCD CONN YOGA3_11"



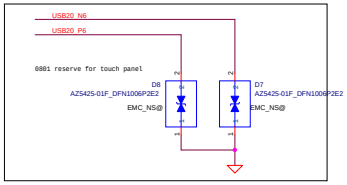
Touch

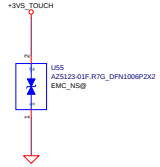




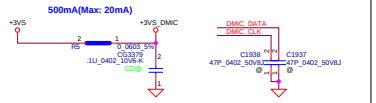
for win8 button wake up

0415 update

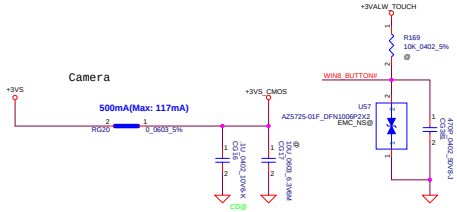




DMIC



Camera



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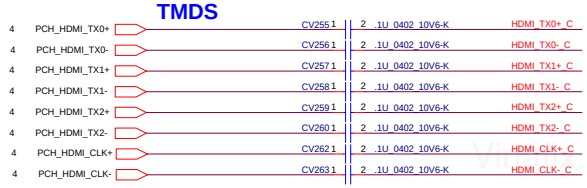
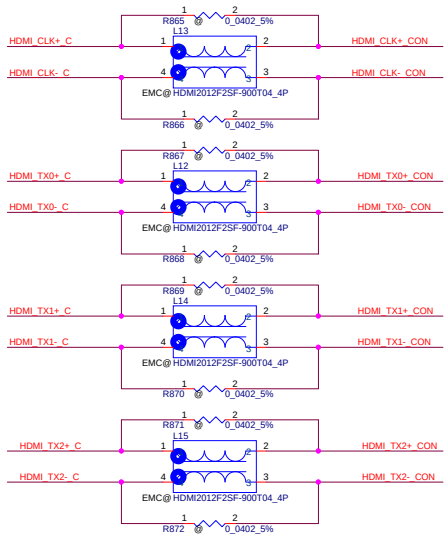
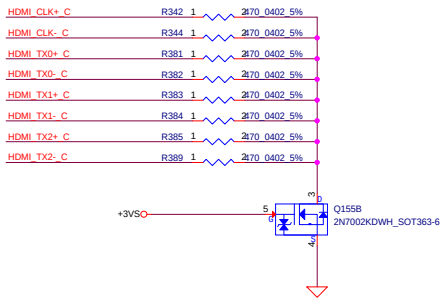
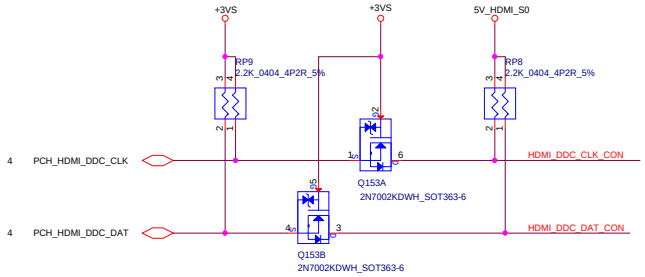
TMDS



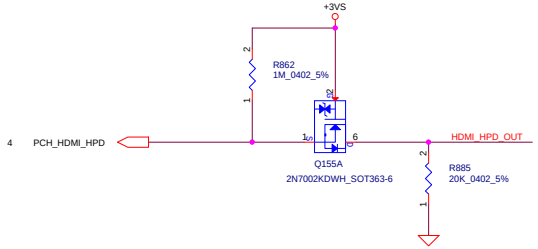




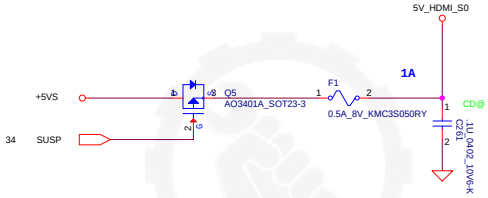
DDC



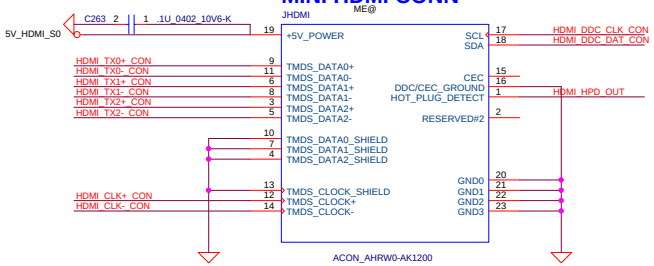
H-PLUG



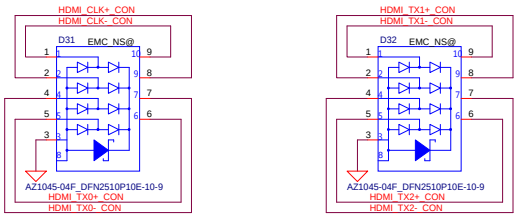
CONN

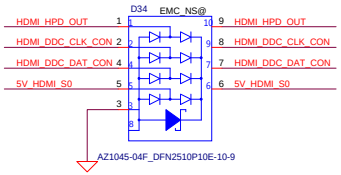


MINI HDMI CONN



ES





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Title: **HDMI**

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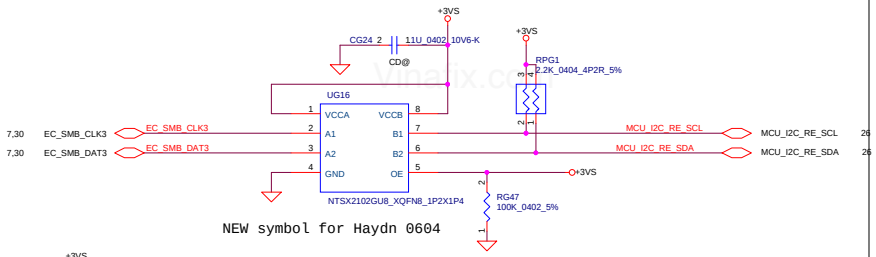
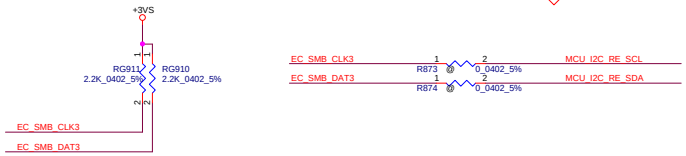
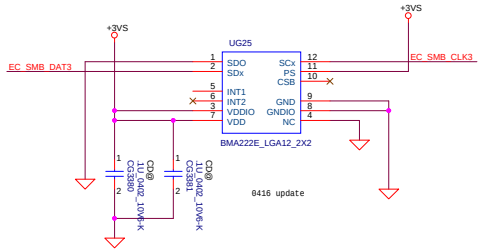


NEW symbol for Haydn 0604

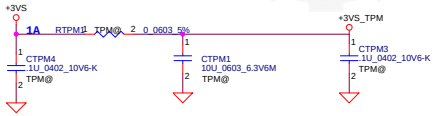


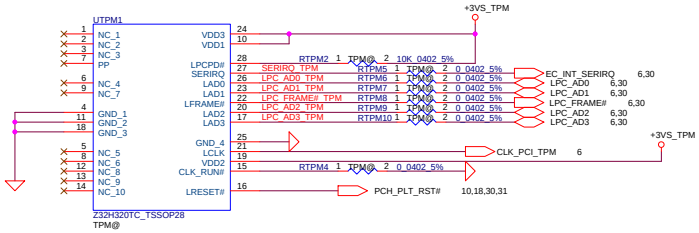
When use ISH change RG911/RG910 to 1K

G-SENSOR



TPM





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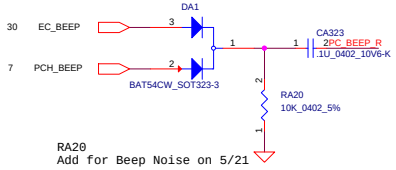
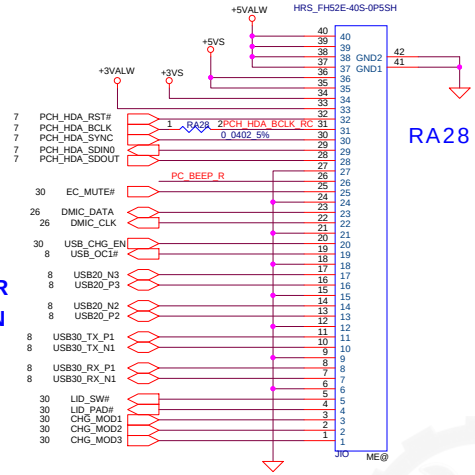
JIO HDA CARDREADER USB CONN

Vinafix.com



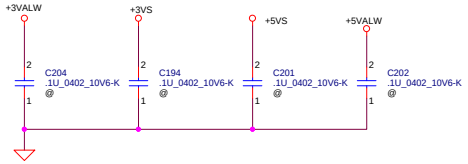
RA20
Add for Beep Noise on 5/21

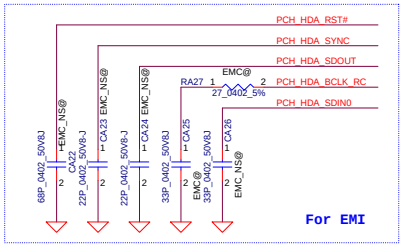


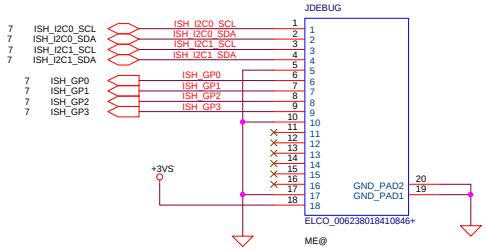
RA28 Close to JIO

CARD READER
Left USB_CONN

NEW symbol for Haydn 0609







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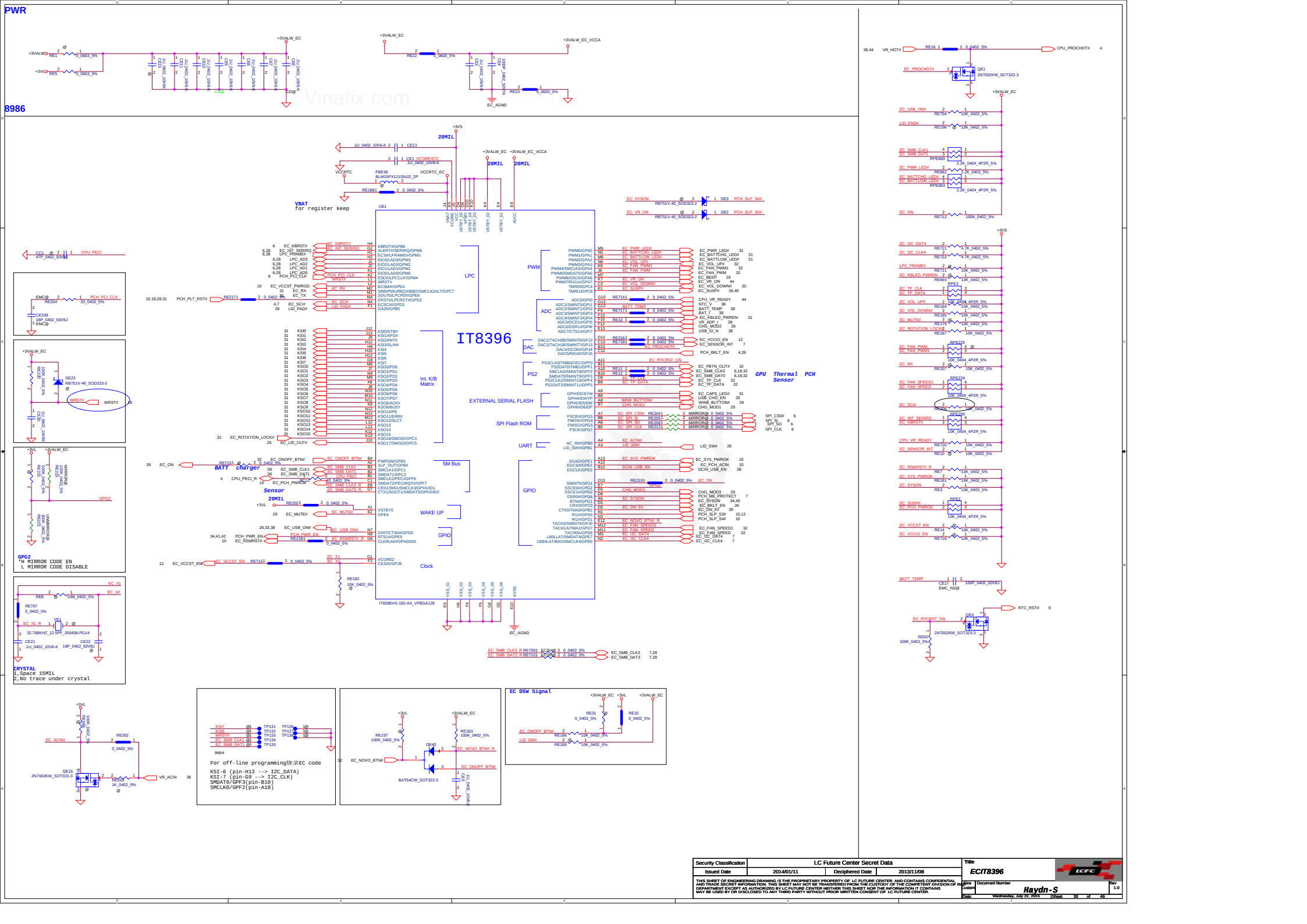
Title: **AUDIO**

Size: C | Document Number: **Haydn-S** | Rev: 1.0

Date: Wednesday, July 22, 2015 | Sheet 29 of 46



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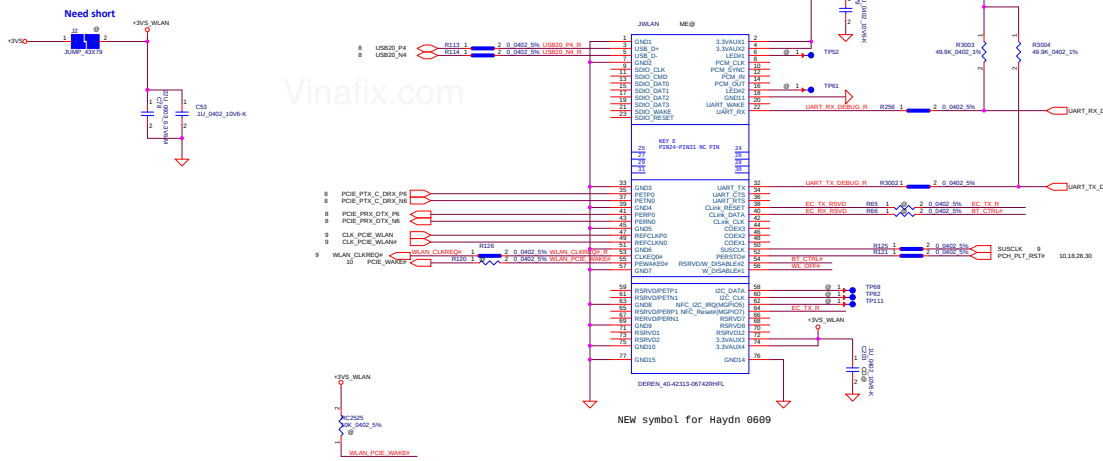
Title: ECIT8396

Size: Custom | Document Number: Haydn-S | Rev: 1.0

Date: Wednesday, July 22, 2015 | Sheet 30 of 46

WIFI&BT Board Connector

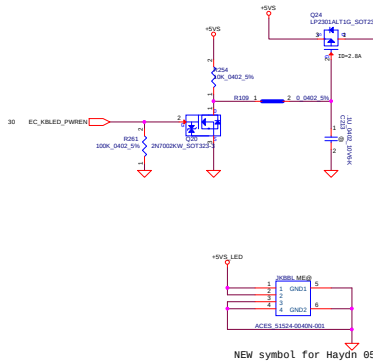
Mini Card(WLAN/WiMAX)

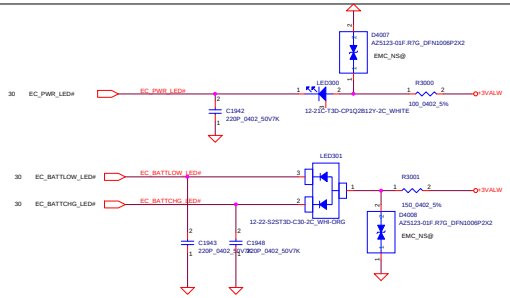


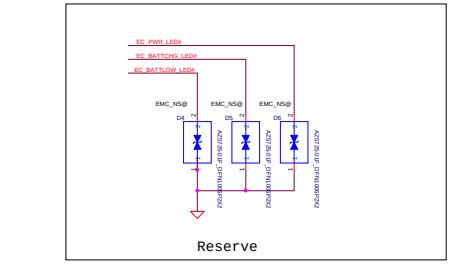
WLAN&BT Combo module circuits

	BT on module Enable	BT on module Disable
* BT_CRTL	H	L
PCH_BT_ON#	L	H

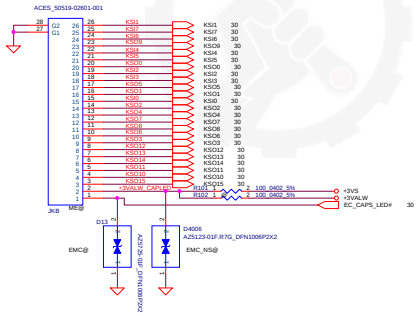
KB BL







Keyboard Connector



+3VALW_CAPLED	C117	1	2 EMC_NS@ 100P_0402_50VBJ	EC_CAPS_LED#	C133	1	2 EMC_NS@ 100P_0402_50VBJ
KSO2	C89	1	2 EMC_NS@ 100P_0402_50VBJ	KSO1	C90	1	2 EMC_NS@ 100P_0402_50VBJ
KSO15	C92	1	2 EMC_NS@ 100P_0402_50VBJ	KSO7	C93	1	2 EMC_NS@ 100P_0402_50VBJ
KSO6	C94	1	2 EMC_NS@ 100P_0402_50VBJ	KSI2	C95	1	2 EMC_NS@ 100P_0402_50VBJ
KSO8	C96	1	2 EMC_NS@ 100P_0402_50VBJ	KSO5	C97	1	2 EMC_NS@ 100P_0402_50VBJ
KSO13	C98	1	2 EMC_NS@ 100P_0402_50VBJ	KSI3	C99	1	2 EMC_NS@ 100P_0402_50VBJ
KSO12	C100	1	2 EMC_NS@ 100P_0402_50VBJ	KSO14	C109	1	2 EMC_NS@ 100P_0402_50VBJ
KSO11	C119	1	2 EMC_NS@ 100P_0402_50VBJ	KSI7	C110	1	2 EMC_NS@ 100P_0402_50VBJ
KSO10	C107	1	2 EMC_NS@ 100P_0402_50VBJ	KSI6	C122	1	2 EMC_NS@ 100P_0402_50VBJ
KSO3	C116	1	2 EMC_NS@ 100P_0402_50VBJ	KSI5	C108	1	2 EMC_NS@ 100P_0402_50VBJ
KSO4	C115	1	2 EMC_NS@ 100P_0402_50VBJ	KSI4	C123	1	2 EMC_NS@ 100P_0402_50VBJ
KSI0	C121	1	2 EMC_NS@ 100P_0402_50VBJ	KSO9	C111	1	2 EMC_NS@ 100P_0402_50VBJ
KSO0	C124	1	2 EMC_NS@ 100P_0402_50VBJ	KSI1	C120	1	2 EMC_NS@ 100P_0402_50VBJ

For EMC

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Title: CONN(WLAN&KB&PWR&BT)

Size: D | Document Number: Haydn-S | Rev: 1.0

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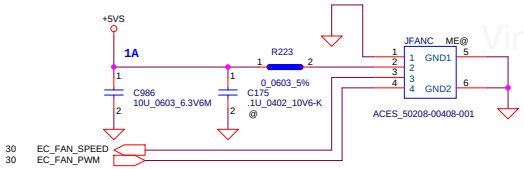
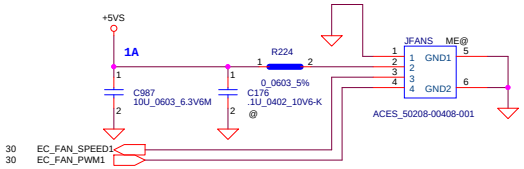
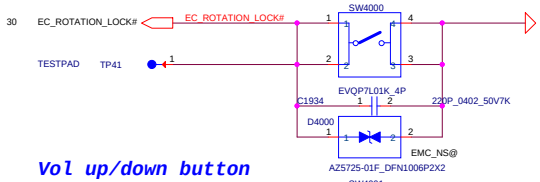
THERMAL SENSOR AND FAN

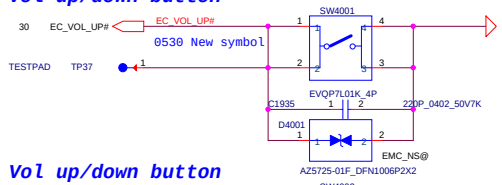




Rotation button



Vol up/down button



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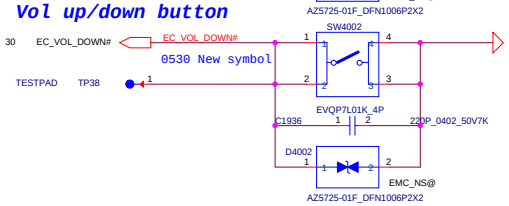
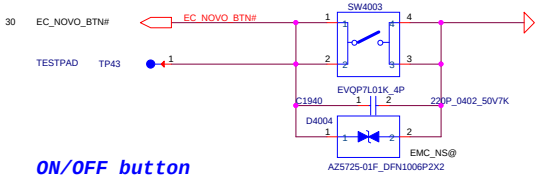
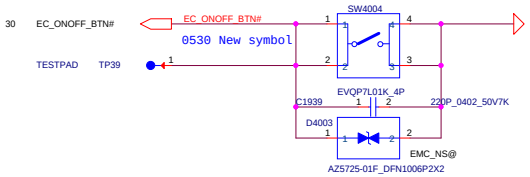


NOVO button

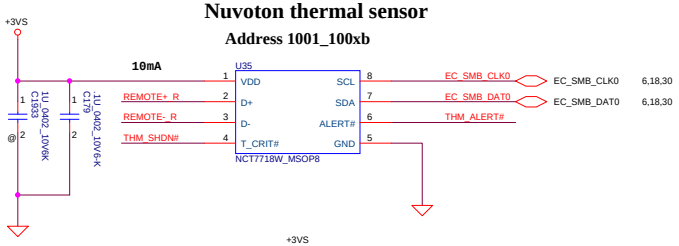


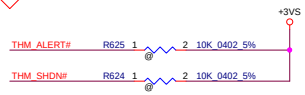
ON/OFF button

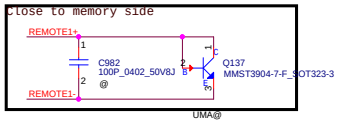


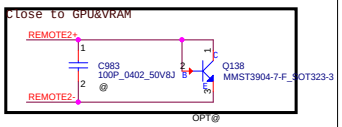
Nuvoton thermal sensor

Address 1001_100xb









REMOTE1+/-:
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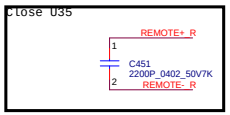
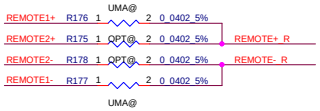
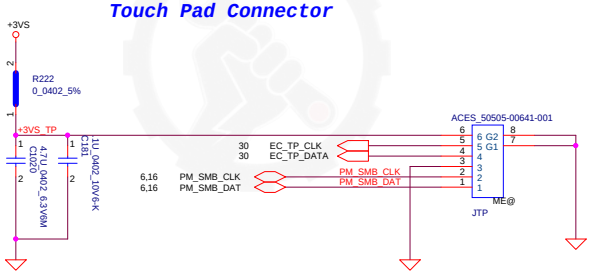
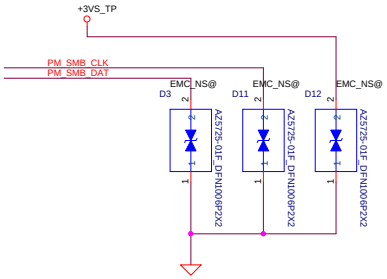
Trace length:<8"





Touch Pad Connector





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Title: CONN(THM&FAN&RTN&SPK)

Size: C | Document Number: Haydn-S | Rev: 1.0

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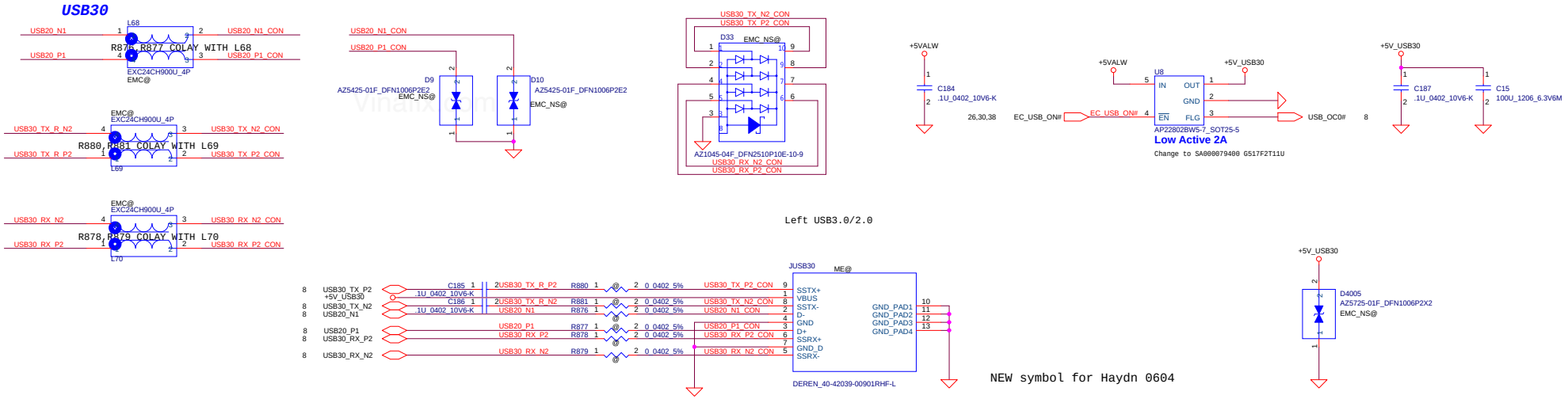

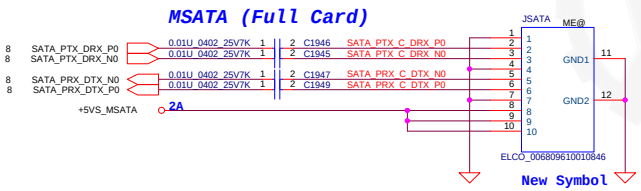

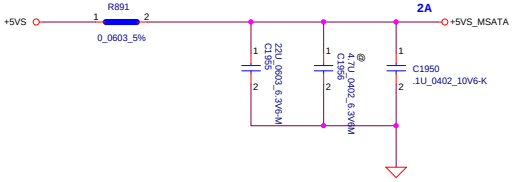

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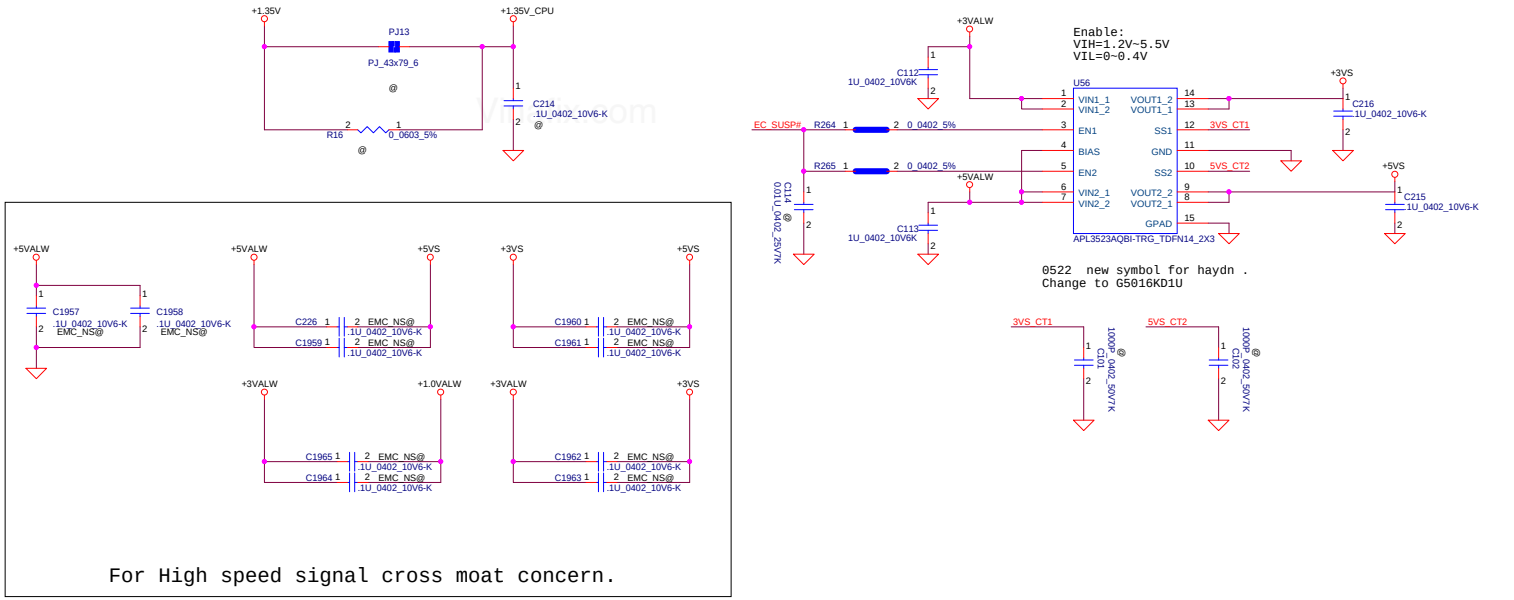
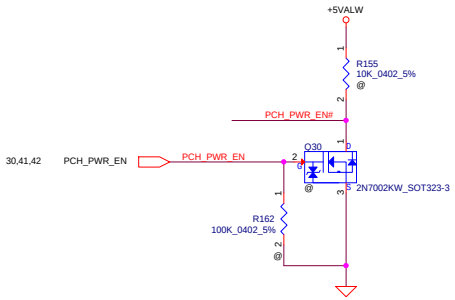
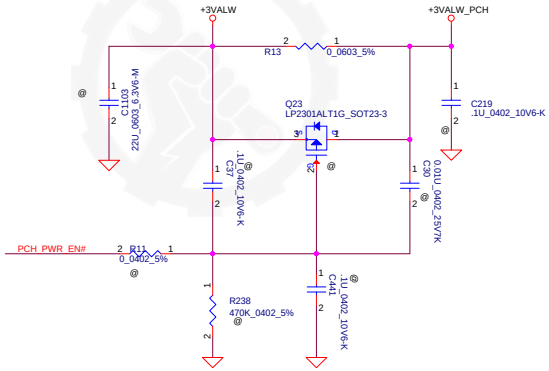
Title: CONN(MSATA&USB30&USB

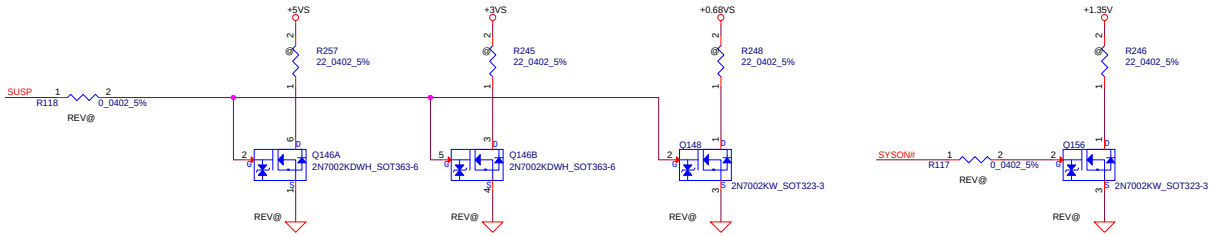
Size: C | Document Number: Haydn-S | Rev: 1.0

Date: Wednesday, July 22, 2015 | Sheet 33 of 46









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Title: **POWER SWITCH**

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FD1 FD2 FD3 FD4 FD5 FD6

0801 DFB需求新增

PAD_CT6P0B7P0D3P6

H1 HOLEA — PAD_CT6P0B7P0D3P6
H12 HOLEA — PAD_CT6P0B7P0D3P6
H14 HOLEA — PAD_CT6P0B7P0D3P6
H15 HOLEA — PAD_CT6P0B7P0D3P6
H16 HOLEA — PAD_CT6P0B7P0D3P6

PAD_CT6P0

H2 HOLEA — PAD_CT6P0
H4 HOLEA — PAD_CT6P0
H5 HOLEA — PAD_CT6P0

PAD_C7P0D4P3

H3 HOLEA — PAD_C7P0D4P3
H6 HOLEA — PAD_C7P0D4P3
H10 HOLEA — PAD_C7P0D4P3

PAD_RT4P0X2P0

H18 HOLEA — PAD_RT4P0X2P0
H19 HOLEA — PAD_RT4P0X2P0

PAD_C7P0D5P6

H11 HOLEA — PAD_C7P0D5P6

PAD_C7P0D2P3

H7 HOLEA — PAD_C7P0D2P3
H9 HOLEA — PAD_C7P0D2P3
H13 HOLEA — PAD_C7P0D2P3

PAD_CT7P0ShapeB7P0X8P25D2P3

H17 HOLEA — PAD_CT7P0ShapeB7P0X8P25D2P3

PAD_ShapeT6P0X5P5

H20 HOLEA — PAD_ShapeT6P0X5P5

PAD_O2P7X2P2D2P7X2P2N

H21 HOLEA — PAD_O2P7X2P2D2P7X2P2N

PAD_C2P2D2P2N

H22 HOLEA — PAD_C2P2D2P2N

SH1 ME@ — SPRING_FINGER_6.2X1.64
SH2 ME@ — SPRING_FINGER_6.2X1.64
SH3 ME@ — SPRING_FINGER_6.2X1.64

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Title: **Screw and Hole**

Size: C | Document Number: **Haydn-S** | Rev: 1.0

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SDV

1/19:
1.Firstly initial

1/21:
1.PCH ISH reserve sensor solution

1/22:
1.U8 USB power switch change to AP22802BW5-7_SOT25-5
from AP2820CMMTR-G1_MSOP8

1/28:
1.EC change to IT8986 from IT8386

2/4
1.EC_ON change to GPJ1
2.GPU 1.05VGS source change to +1.0VALW
3.BAT_I change to GPI3
4.CPU_VR_READY change to GPI0
5.EC_VR_ON change to GPA7
6.EC_VCCIO_EN change to GPJ2
7.VGA_AC_DET change to GPJ3
8.VGA 1.05VGS HW load switch del

2/9
1.Add VDDQ_PGOOD to EC GPJ3

2/10
1.RC138,QC6,RC136 change to unmount
2.RC1599 change to mount
3.U9 change to AP22802AW5-7_SOT25-5 from AP2821KTR-G1_SOT23-5

2/11 **
1.Add SH1/SH2/SH3 shielding
2.RC1585 unmount,RC1586 mount

2/12
1.Del C224/C225/C217/C218/C226/C220
2.RC157/RC170 change to unmount
3.Del PR138,Add PR1015/PR1016
4.Del PD109/PD110 Add PD111
5.Add PR1017

2/13
1.Del TP203/TP172/TP173/TP177/TP178
2.Del UC8/RC1591/DC2/CC1247/JC2/CC1248
3.Del UC7/RC1590/DC3/CC1245/RC1592/CC1246
4.QC12/QC16 change to AO5804EL_SC89-6 from 2N7002KDWH_SOT363-6
5.QC13/QC14 change to DMG1012T-7_SOT523-3 from 2N7002KW_SOT323-3

2/24
1.JDDRL.181 change to DDRA_DQ56 from DDRA_DQ61
2.JDDRL.180 change to DDRA_DQ61 from DDRA_DQ56
3.JDDRL.191 change to DDRA_DQ62 from DDRA_DQ59
4.JDDRL.192 chnage to DDRA_DQ58 from DDRA_DQ62
5.JDDRL.194 change to DDRA_DQ59 from DDRA_DQ58
6.RC59 change to @

2/25
1.Add JDEBUG connector for Intel ISH debug
2.VRAM Hynix change to H5TC4G63CFR-N0C
3.VRAM Samsung change to K4W4G1646E-BC1A
4.CC165 change to @
5.CC57 change to 1uf from 0.1uf and mount
6.U56 VIN1/VIN2,VOUT1/VOUT2 swap

2/28
1.Del TP197,TP198,TP200,TP40,TP141,TP44,TP189,TP191,TP196,
TP183,TP185,TP184,TP181,TP194,TP187,TP182,TP188,TP193,TP190,TP192,TP201,TP195,TP186,TP236

3/2 *****
1.Del RC1596,RC1597,Add RPC68
2.Change RPC4 to 10K_0404_4P2R_5% from 10K_0804_8P4R_5%
3.Change UV2 to 74LVC1G08SE-7_SOT353-5 from 74LVC1G08GW_SOT353-1-5

3/3
1.JDEBUG change to ELCO_006238018410846+
2.Reserve RE720 for CPU_VR_READY pull high +3VS
3.UTPM1 change to Z32H320TC_TSSOP28 from ST33ZP24AR28PVSP_TSSOP28
4.RTPM2 change to 10K from 4.7K
5.Del RE214/RE215/RE708,Del RE690/RE691@
6.Add RE721/RE722 10K pull high +3VS
7.Del VDDQ_PGOOD Add EC_SENSOR_INT
8.WIN8_BUTTON# change to EC PIN A8, CHG_MOD1 change to EC PIN B7
9.Add EC_I2C_DAT4 to EC PIN M3, Add EC_I2C_CLK4 to EC PIN N2
10.Add RPC69/RC2533/RC2534/QC45

3/4
1.RE10 pin2 change to EC_SENSOR_INT from EC_ON_5V
2.Update JDEBUG symbol
3.Reserve CC1255, C1957/C1958/C226/C1959/C1960/C1961/C1962/C1963/C1964/C1965 for EMC

3/5
1.Del TP90/TP92

3/9
1.Add RC2535 0ohm, Add RC2536 1K to GND

3/10
1.H17 change to PAD_CT7P0ShapeB7P0X8P25D2P3 from PAD_C7P0D2P3

3/11
1.RC64 change to @ from ES@
2.CC23 change to @

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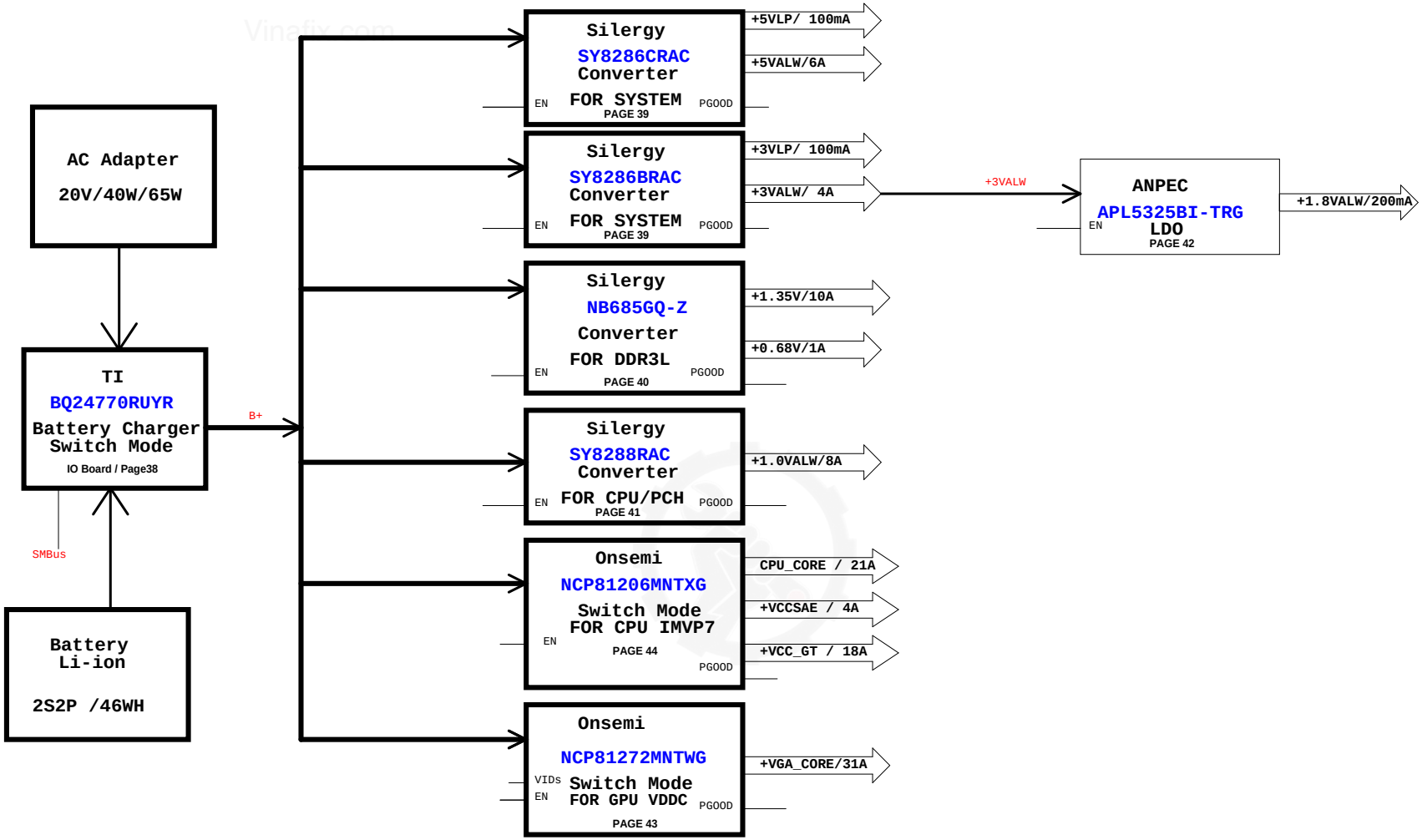

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Issued Date	2014/01/11	Deciphered Date	2013/11/08

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Title: PWR_BLOCK DIAGRAM

Size: C | Document Number: Haydn-SKL | Rev: 1.0

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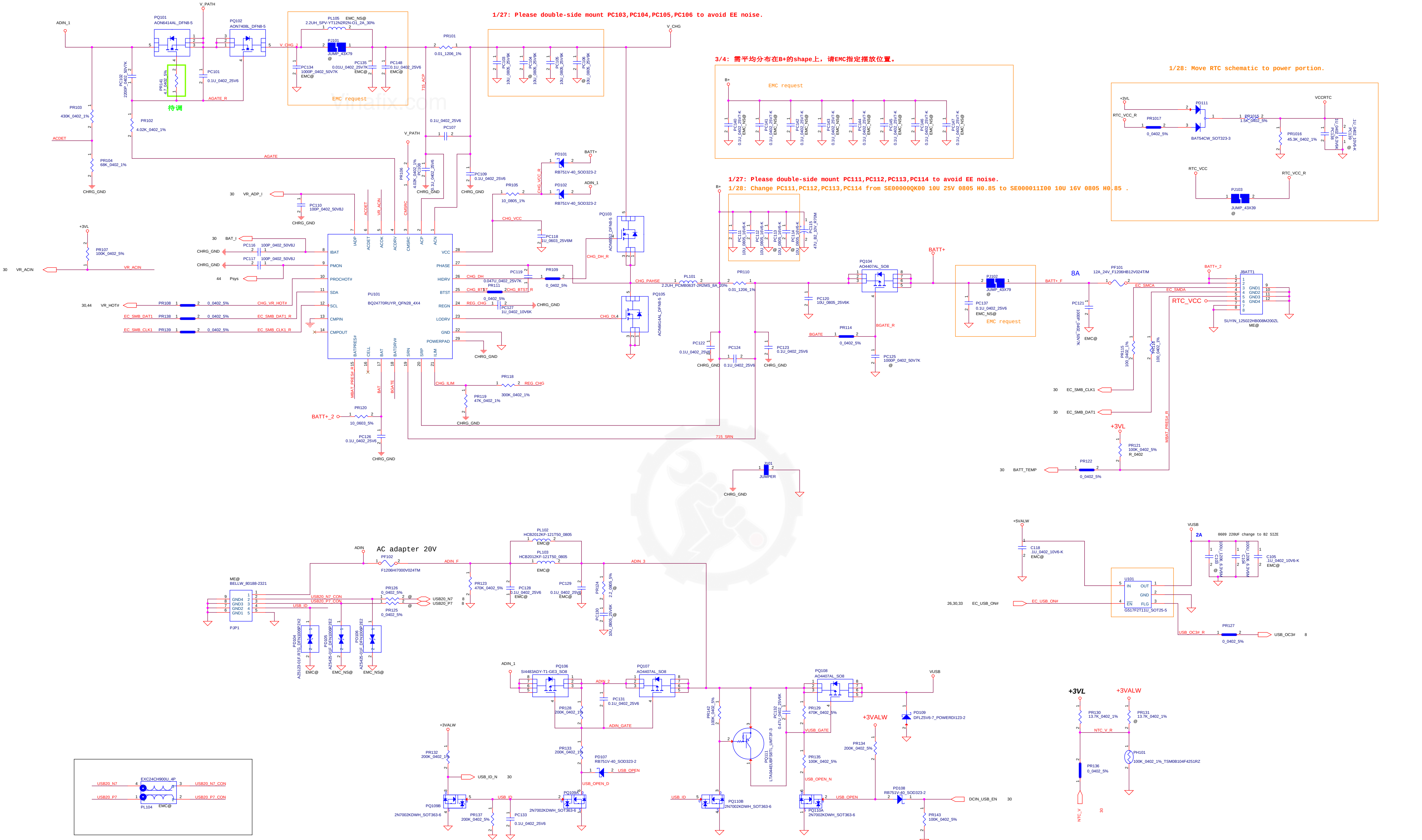

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Issued Date	2014/01/11	Deciphered Date	2013/11/08

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Title: PWR_NVDC Charger

Size	Document Number	Rev
D	Haydn-SKL	1.0

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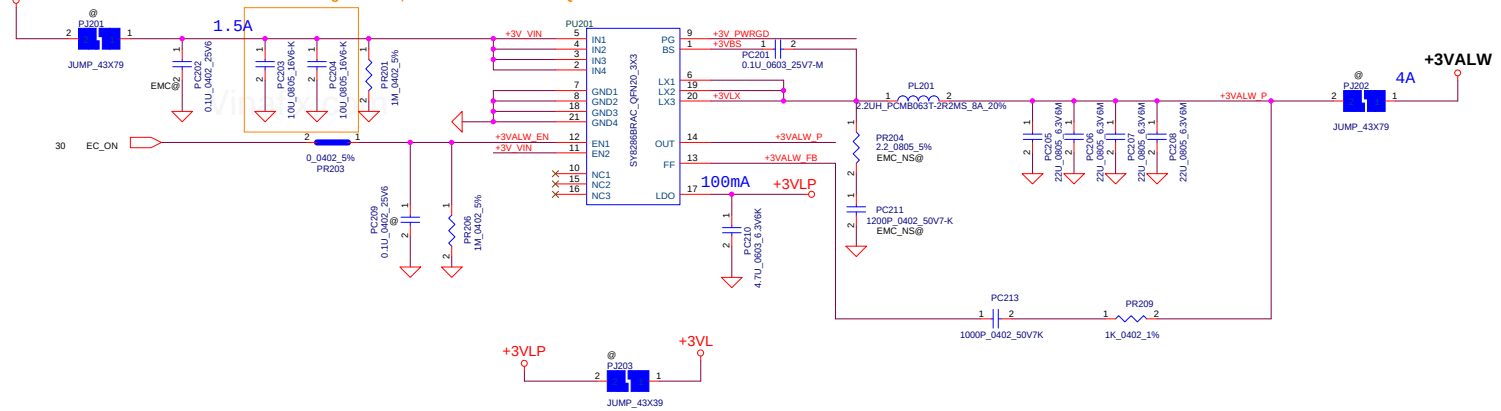
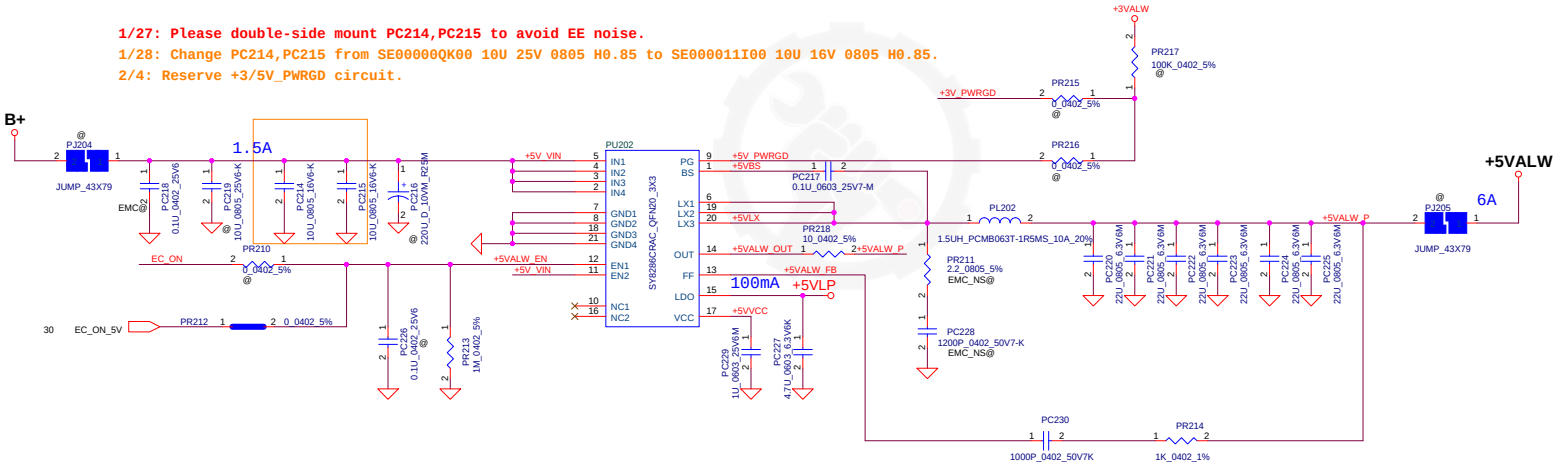
1/27: Please double-side mount PC203,PC204 to avoid EE noise.
1/28: Change PC203,PC204 from SE00000QK00 10U 25V 0805 H0.85 to SE000011I00 10U 16V 0805 H0.85 .



1/27: Please double-side mount PC214,PC215 to avoid EE noise.
1/28: Change PC214,PC215 from SE00000QK00 10U 25V 0805 H0.85 to SE000011I00 10U 16V 0805 H0.85.
2/4: Reserve +3/5V_PWRGD circuit.



3VALWP VFB=2V TDC 5A Fsw=350KHZ OCP:7.8A~9.5A	5VALWP TDC 5A Fsw=300KHZ OCP:7.8A~9.5A

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Issued Date	2014/02/20	Deciphered Date	2014/02/20

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Title: PWR_3VALWP/5VALWP

Size: C | Document Number: Haydn-SKL | Rev: 1.0

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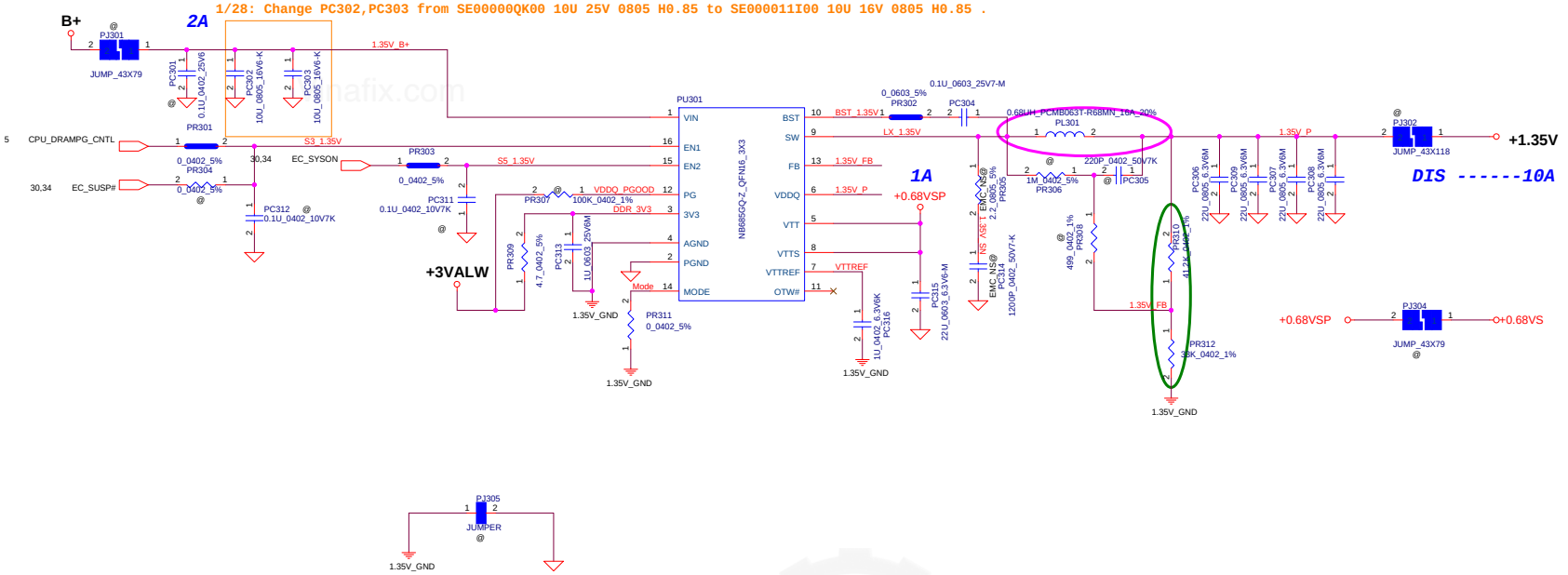
1/27: Please double-side mount PC302,PC303 to avoid EE noise.
1/28: Change PC302,PC303 from SE00000QK00 10U 25V 0805 H0.85 to SE000011I00 10U 16V 0805 H0.85 .



+1.35VP
Vout=1.367V
Iocp min=13A fro DIS SKU
Iocp min=6A fro UMA SKU

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Issued Date	2014/01/11	Deciphered Date	2013/11/08

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Title: PWR_1.35V/0.68VS

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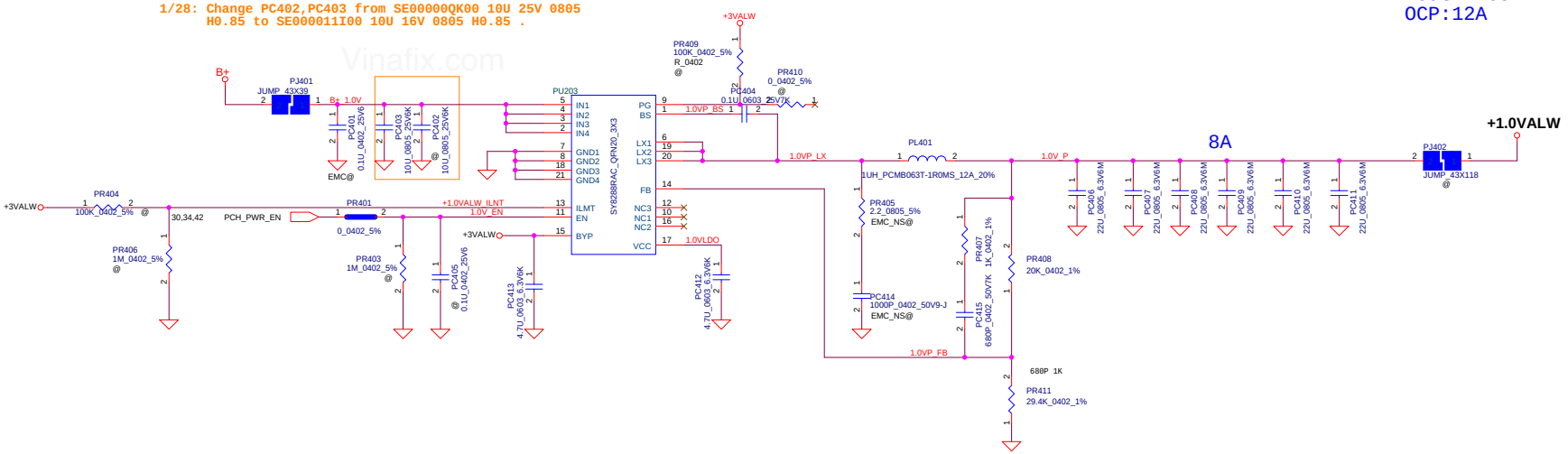
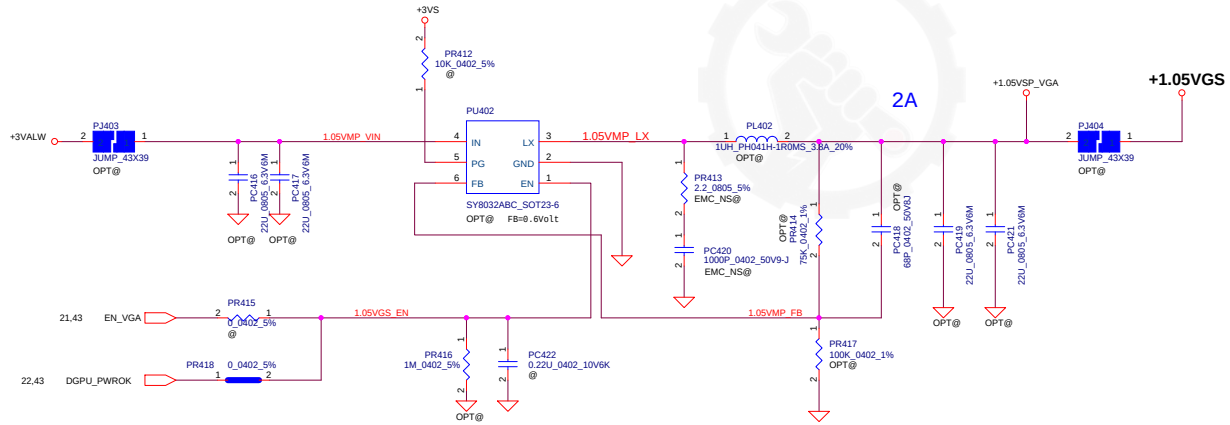
1/27: Please double-side mount PC402,PC403 to avoid EE noise.

1/28: Change PC402,PC403 from SE00000QK00 10U 25V 0805 H0.85 to SE000011I00 10U 16V 0805 H0.85 .

Fsw=800KHZ
Vfb=0.6V
Vout=1.051V
OCP:12A





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Issued Date	2014/01/11	Deciphered Date	2013/11/08

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Title: PWR_1.0VALW/1.05VGS

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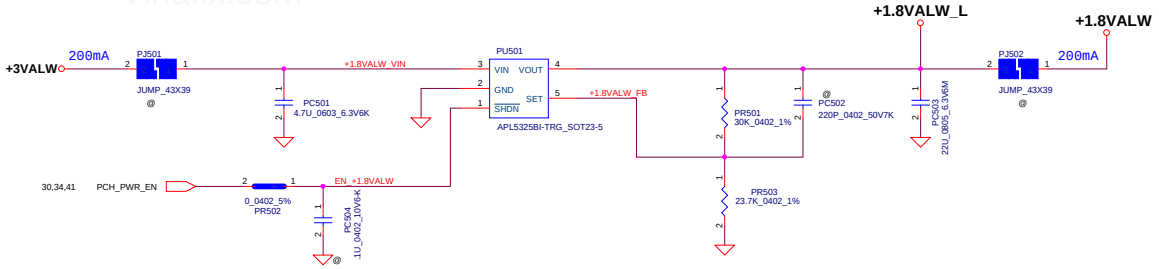

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Title: **PWR_+1.8VALW**

Size: Custom | Document Number: **Haydn-SKL** | Rev: 1.0

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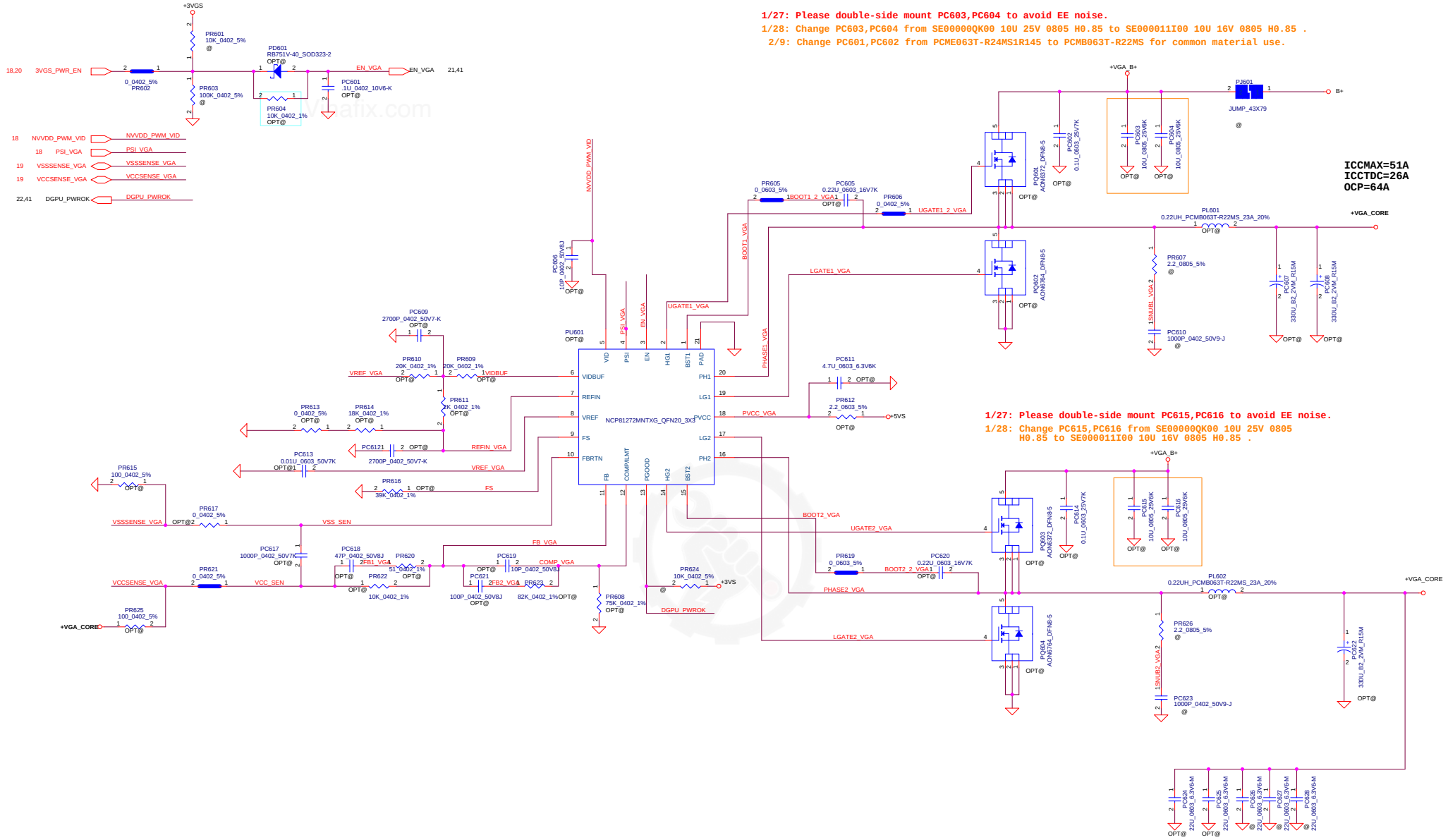
1/27: Please double-side mount PC603,PC604 to avoid EE noise.
1/28: Change PC603,PC604 from SE00000QK00 10U 25V 0805 H0.85 to SE000011I00 10U 16V 0805 H0.85 .
2/9: Change PC601,PC602 from PCME063T-R24MS1R145 to PCMB063T-R22MS for common material use.

ICCMAX=51A
ICCTDC=26A
OCP=64A

1/27: Please double-side mount PC615,PC616 to avoid EE noise.
1/28: Change PC615,PC616 from SE00000QK00 10U 25V 0805 H0.85 to SE000011I00 10U 16V 0805 H0.85 .



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Issued Date	2014/01/11	Deciphered Date	2013/08/05

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Title: PWR-VGA_CORE

Size: Custom | Document Number: Haydn-SKL | Rev: 1.0

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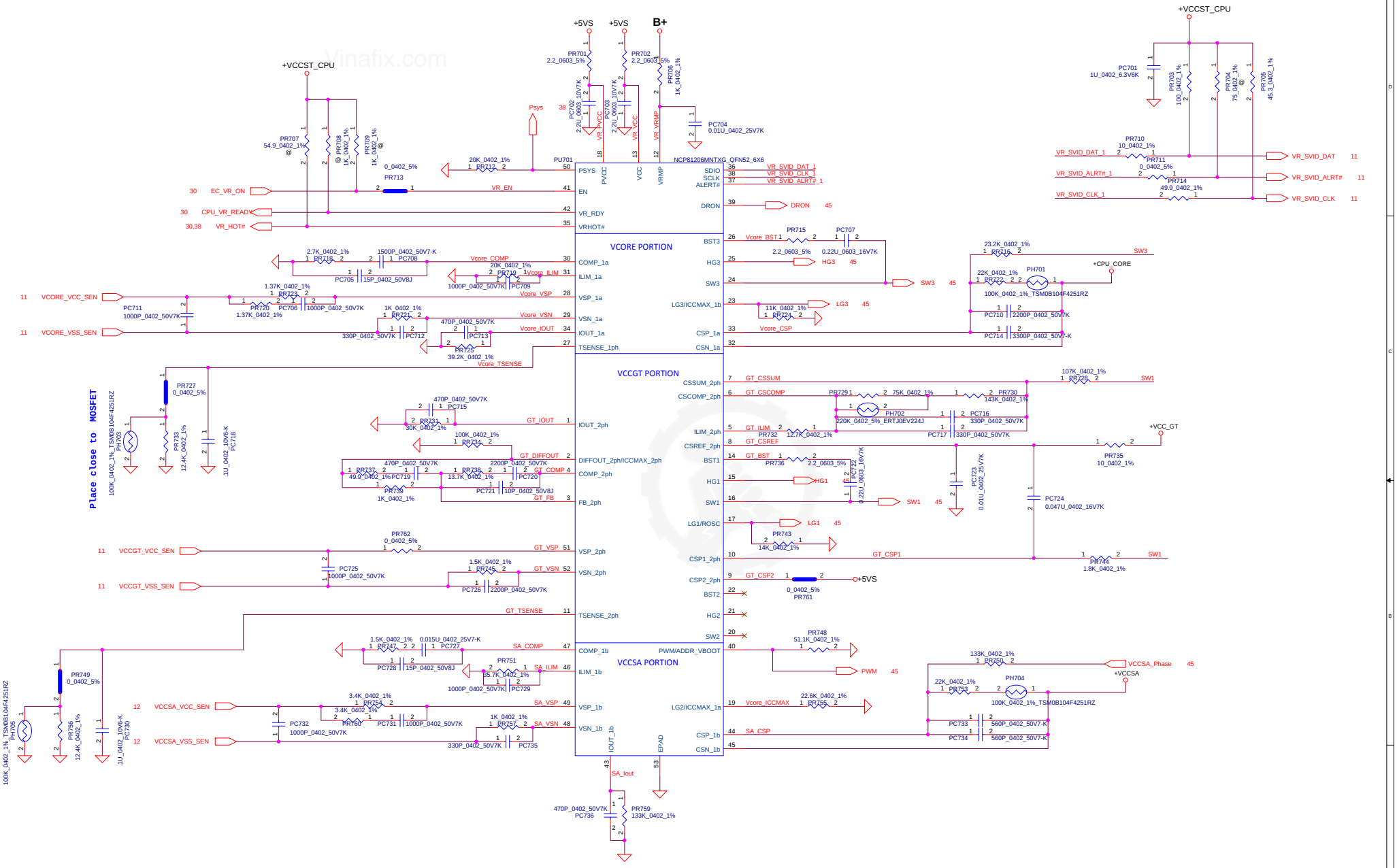

Security Classification	LC Future Center Secret Data		
Issued Date	2012/09/03	Deciphered Date	2012/09/03

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Title: PWR_CPU_CORE

Size: C | Document Number: Haydn-SKL | Rev: 1.0

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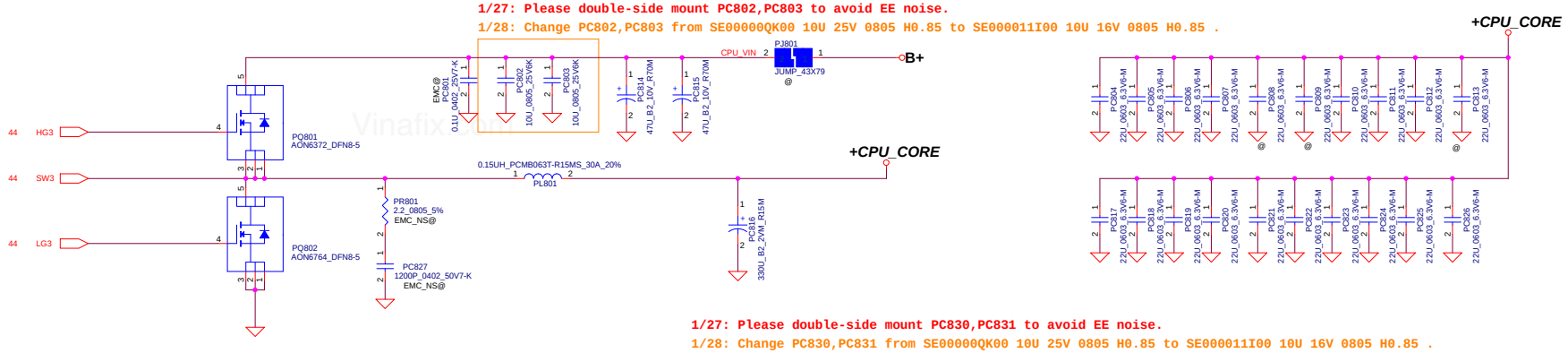
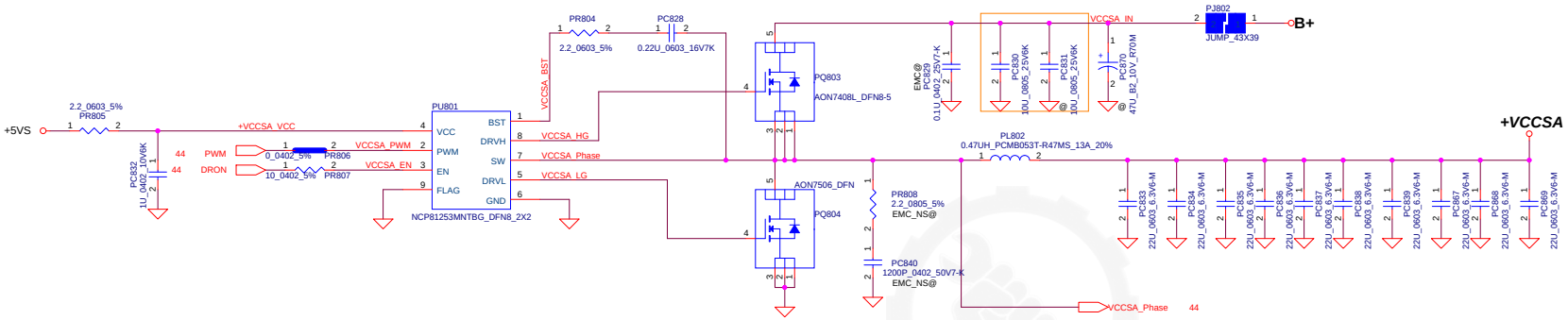
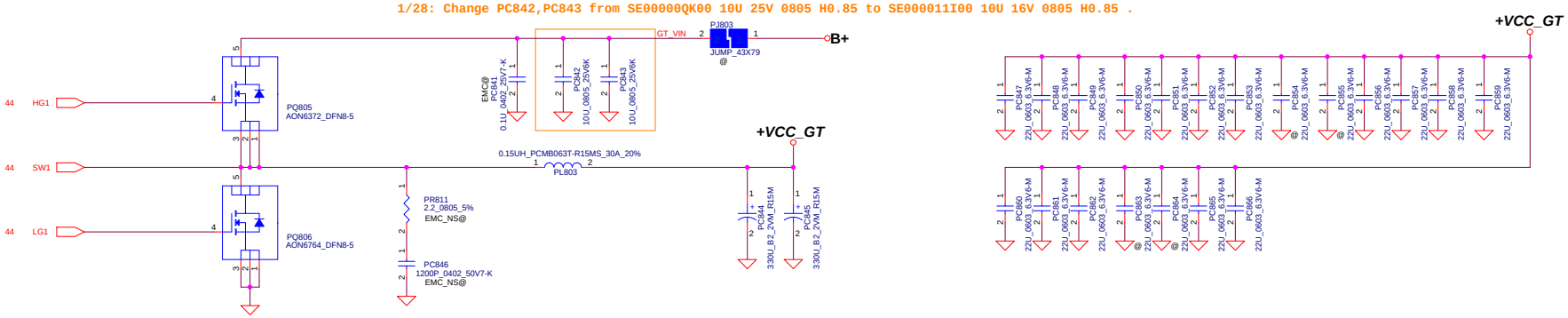
1/27: Please double-side mount PC802,PC803 to avoid EE noise.
1/28: Change PC802,PC803 from SE00000QK00 10U 25V 0805 H0.85 to SE000011I00 10U 16V 0805 H0.85 .



1/27: Please double-side mount PC830,PC831 to avoid EE noise.
1/28: Change PC830,PC831 from SE00000QK00 10U 25V 0805 H0.85 to SE000011I00 10U 16V 0805 H0.85 .
2/9: Change PC802 from PCMB063T-R47MS to PCMB053T-R47MS for layout limit.



1/27: Please double-side mount PC842,PC843 to avoid EE noise.
1/28: Change PC842,PC843 from SE00000QK00 10U 25V 0805 H0.85 to SE000011I00 10U 16V 0805 H0.85 .



Security Classification	LC Future Center Secret Data		
Issued Date	2013/11/08	Deciphered Date	2013/11/08

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Title: PWR_CPU_Core

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Title

PWR_Change list

Size	Document Number	Rev
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